A Direct Power Conversion Topology for Grid Integration of Hybrid AC/DC Energy Resources

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***Abstract*—This paper proposes a multiple-input versatile matrix converter (VMC) for integrating hybrid ac/dc energy resources and storages to the power grid. The VMC is developed from the traditional indirect matrix converter but operates in the reverse-boost mode rather than in the forward-buck mode. The reverse-boost mode is more relevant here since most renewable sources and energy storages have lower voltages than the grid. The eventual VMC developed uses an alternative nine-switch converter, rather than usual six-switch voltage-source converter, for providing six input terminals in total. One three-phase ac source and three dc sources, or other source combinations, can therefore be connected to the VMC. Powers from these sources are channeled to the three-phase utility grid through the VMC's current-source inverter. Their proper dispatches are guaranteed by the proposed control and modulation schemes, which also help maintain near-sinusoidal input and output current waveforms. Mathematical proofs, simulation, and experimental results have shown that the VMC can indeed operate as intended.**

***Index Terms*—Direct power conversion, grid integration, hybrid ac/dc resources, versatile matrix converter (VMC).**

I. Introduction

INTEREST in distributed generation and microgrids has led to the widespread integration of energy resources and energy storage systems to the utility grid. Broadly, these energy resources and storages can be categorized under the ac or dc types. Examples for the ac type include wind energy conversion system, diesel generator, microturbine, flywheel energy storage system, and other systems driven by electric machines. The dc type, on the other hand, seldom involves electric machines. It covers mostly static sources and storages like the photovoltaic (PV) panel, fuel cell, battery, and ultracapacitor [1]. Among the two types, those with renewable natures like PV and wind power plants are uncontrollable. Their outputs are mostly decided by the prevailing weather conditions which include wind speed and solar irradiation level [2]. High penetration of renewable sources might therefore lead to intermittent and uncertain voltage and frequency fluctuations in the grid.

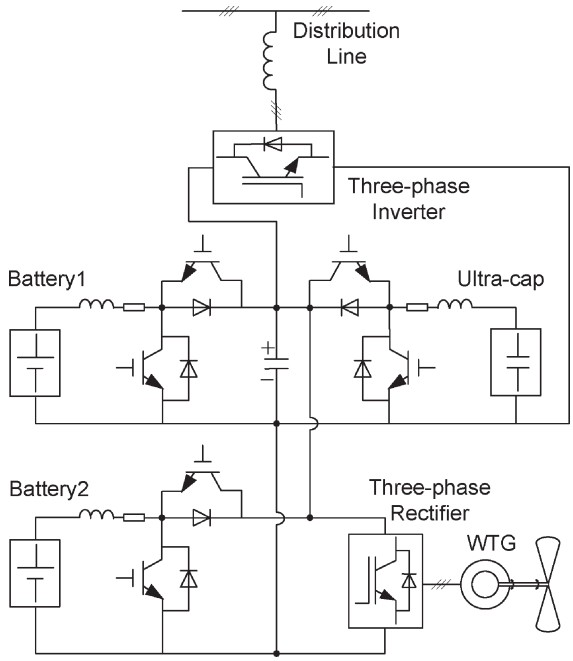

Fig. 1. Circuit layout showing grid integration of hybrid wind/battery/ultracapacitor resources.

To smoothen out these fluctuations, different renewable sources can be integrated together, whose characteristics must complement each other to produce a more stable output power. For even higher level of certainty and to better meet grid codes, controllable energy storages and/or dispatchable generators can also be added to the system [3]–[9]. Such integration would usually require some power converters to be added like the back-to-back ac/dc/ac converter found with a wind generator and the dc/dc boost plus dc–ac inverter found with a PV source [10], [11]. If both wind and PV sources are present, they can either retain their independent power converters or merge some parts to save components. For the latter, one possibility is for the sources to share a single common grid-side inverter, which might, at times, be underutilized if only a single source is tied to it. The remaining front-end ac/dc and dc/dc converters tied directly to the sources (or storages) would remain unchanged.

To illustrate, Fig. 1 shows an example system, where multiple hybrid resources are tied to the grid. It shows a wind turbine, battery storages, and ultracapacitor tied to a common dc bus

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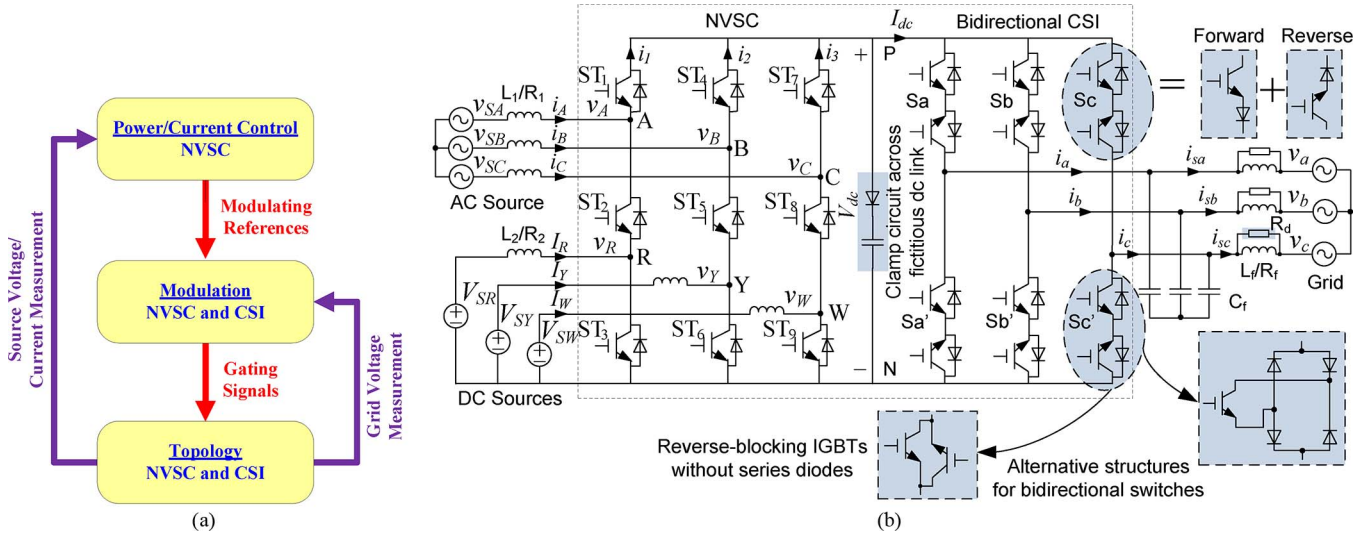

Fig. 2. Proposed VMC system with one three-phase ac and three dc energy sources—(a) Overview and (b) VMC topology.

through their separate ac/dc and dc/dc power converters. The common dc bus is then tied to a common dc/ac inverter for grid integration. No doubt, this is a straightforward and well-known practice. References [12] and [13] subsequently merge more power converters to gain 25% saving in semiconductors. The resulting system still needs a dc-link electrolytic capacitor for creating two power conversion stages. This capacitor may cause premature failure and can increase the size of the overall converter. It may require sensor and control scheme too for regulating its voltage so as to avoid damages caused by over-voltages. An alternative would be to consider foil capacitor but only when the tradeoffs of higher volume and price for the same capacitance and rating are acceptable.

Avoiding the dc-link capacitor completely is another option, which has long been pursued by those single-stage matrix converters studied in [14]–[28]. Among them, the most attractive would probably be the indirect matrix converter (IMC), whose fictitious rectifier/inverter arrangement makes it highly flexible for topological extension [22]–[28]. The IMC, like other matrix converters, is, however, usually investigated in the forward-buck mode whose input-to-output gain is limited to 0.866. This is surely not suitable for grid integration since voltages from renewable sources and energy storages are usually smaller than the output grid voltage. Reverse-boost mode of operation is therefore more relevant but has seldom been studied, particularly with converter merging pursued simultaneously to save components. It is therefore the theme of this paper to investigate on a versatile matrix converter (VMC) operating in its reverse-boost mode. The purpose is to integrate hybrid ac/dc sources and storages to the grid with the following intended features:

1) integration done with lesser semiconductor switches;
2) passive step-up transformer not needed for grid integration of low-voltage energy resources if isolation is not a concern;
3) accurate power dispatches and near-sinusoidal input and output currents.

Simulation and experimental testing have already confirmed the effectiveness of the overall system.

II. Topology and Modulation

Like most power conversion systems, the proposed VMC system is organized into three blocks named as topology, modulation, and control in Fig. 2(a). Discussion of the system will therefore be in the same format from the bottom up. That means that the topology and modulation will be sequentially discussed in this section first before addressing the control schemes in a later section.

A. Topology

Unlike the usual six-switch voltage-source converter (VSC), the VMC uses a nine-switch VSC (NVSC) [29], [30] and a bidirectional current-source inverter (CSI). Both entities are tied together at their fictitious dc link, as demonstrated in Fig. 2. Six input terminals for connecting to ac/dc sources and three ac output terminals for connecting to the grid are thus formed with the NVSC effectively behaving like a three-phase VSC plus three dc/dc converters. The bidirectional CSI, on the other hand, provides a current path for channeling the extracted powers to the grid or vice versa if the sources are rechargeable like battery, ultracapacitor, and low-speed flywheel.

Switches of the bidirectional CSI must therefore be capable of conducting and blocking in both directions. One way of realizing the switches is to connect two sets of insulated gate bipolar transistors (IGBTs) with series diodes in opposite directions, as highlighted in Fig. 2 for one of the switches. Other arrangements are also shown in Fig. 2, where one possibility is to use reverse-blocking IGBTs for efficiency improvement. The last option might probably be cheaper since it uses only one IGBT and four diodes per switch but can be poorer in efficiency since there are always two series conducting diodes. For safety reasons, a clamp circuit is recommended too like in most matrix converters. It consists of a diode and a small foil capacitor in series at the fictitious dc link. The clamp circuit is usually not operating. It clamps only during abnormal situations like faults, during which the converter has to be turned off. The only path available for the source-side inductive energy to flow is then through the clamp capacitor [24].

TABLE I
SWITCHING STATES AND OUTPUT VOLTAGES OF NVSC

Switching State	ST_1	ST_2	ST_3	V_{AN}	V_{RN}
1	1	1	0	V_{dc}	V_{dc}
2	0	1	1	0	0
3	1	0	1	V_{dc}	0

Referring back to the input NVSC, the observation drawn is that its middle switch ST_2 in the leftmost phase-leg, quoted as an example, is shared by the upper ac/dc and lower dc/dc converters. Such sharing reduces the number of semiconductors by 25% [29], [30] but introduces a switching restriction, as understood from Table I (fourth combination of $V_{\rm AN} = 0$ and $V_{\rm RN} = V_{\rm dc}$ cannot be produced). This restriction, as mentioned in [29] and [30], can be complied if the normalized modulating reference for the lower dc terminal v_{rR} is always placed below that for the upper ac terminal v_{rA}. The sum of v_{rR} and the peak-to-peak of v_{rA}, when placed within the same carrier band of -1–1, will then be equal to or lesser than two.

This is fine for the proposed grid integration, where low modulation indices (translating to high duty ratios for dc/dc converters) are needed for boosting lower voltages from the input sources and storages to the higher grid voltage. The terminal voltages of dc-type storages like battery and ultracapacitor are comparatively low due to their manufacture limitations. Therefore, low modulation indices are expected to produce high boost gains for dc/dc converters. It is nonetheless still a restriction in terms of the input voltage variation range. This can better be illustrated by comparing the IMC and VMC. The IMC uses the usual six-switch VSC with three input ac terminals. To add three more dc terminals, a second six-switch converter can be added in parallel to the fictitious dc link. For each converter, its normalized input peak-to-peak amplitude can vary from zero to two, but for the VMC, the ac or dc peak-to-peak amplitude is always lesser than two if both amplitudes are nonzero. The chosen source maximum amplitude must hence be lowered accordingly. If this limitation is acceptable for the applications under consideration, the proposed VMC would be a suitable grid-tied topology, whose conditioned input and output current waveforms are guaranteed by the modulation schemes to be described next.

B. Modulation of CSI

The output CSI shown in Fig. 2 can, in theory, impose a selected line voltage across the fictitious dc link. The voltage chosen depends on which of the six active and three null states are entered by the CSI. The nine switching states are shown in Fig. 3, where only the on switches of the active states are shown. The null states are not used here, which indirectly means that the modulation index of the CSI cannot be adjusted for voltage-boosting purposes. Instead, the CSI is tasked to only invert the dc-link current to a set of three-phase sinusoidal grid currents. This arrangement can help simplify the overall modulation scheme while preserving the VMC voltage-boosting ability. The latter is guaranteed by adjusting modulation indices of the NVSC connected directly to the sources.

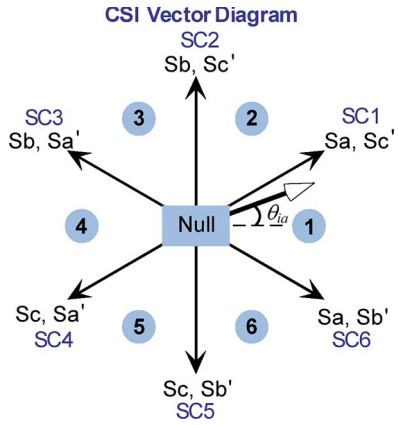

Fig. 3. Space-vector representation of CSI.

Taking sextant $1(-\pi/6 \le \theta_a \le \pi/6)$ of the CSI in Fig. 3 as an example, either voltage v_{ab} or v_{ac} can be imposed across the fictitious dc link depending on whether SC6 or SC1 is entered. Regardless of which state is entered though, upper switch Sa will always be turned on to clamp phase a to the positive dc rail for the whole sextant 1. Choosing SC6 or SC1 will only cause the lower switch Sb′ or Sc′ to turn on alternately, tying their respective phases to the negative dc rail. The same interpretation can be applied to the other five sextants with only a minor difference observed for the even-numbered sextants. To be precise, the even-numbered sextants have a phase clamped to the negative dc rail instead of the positive dc rail.

At any instant, the sextant considered is decided by a reference phasor, whose phase orientation θ_{ia} in Fig. 3 is synchronized with the measured grid voltage after adding in the desired output power factor angle ϕ_o. To guarantee that the fictitious dc-link voltage does not drop below zero, ϕ_o must be set within the range of $-\pi/6$ to $\pi/6$ [35]. With this condition ensured, corresponding active duty ratios d_{o1} and d_{o2} of the CSI can be determined after defining the following set of three-phase normalized current references (m_a, m_b, and m_c):

$$\begin{aligned}
&v_a = V_{om}\cos\theta_{va} \quad v_b = V_{om}\cos\theta_{vb} \quad v_c = V_{om}\cos\theta_{vc}\\
&\theta_{va} = \omega_o t + \varphi_v \quad \theta_{vb} = \theta_{va} - 2\pi/3 \quad \theta_{vc} = \theta_{va} + 2\pi/3\\
&m_a = \cos\theta_{ia} \qquad m_b = \cos\theta_{ib} \qquad m_c = \cos\theta_{ic}\\
&\theta_{ia} = \theta_{va} + \varphi_o \quad \theta_{ib} = \theta_{ia} - 2\pi/3 \quad \theta_{ic} = \theta_{ia} + 2\pi/3 \qquad (1)
\end{aligned}$$

where V_{om} and ω_o are the grid phase voltage amplitude and angular frequency, θ_{va}, θ_{vb}, and θ_{vc} are the grid voltage angles, and θ_{ia}, θ_{ib}, and θ_{ic} are the current reference angles. Power factor angle ϕ_o can then be represented by the phase difference between θ_{ia} and θ_{va}, if the effect from the L_fC_f filter in Fig. 2 is ignored.

Noting next that the sum of m_a, m_b, and m_c is zero, d_{o1} and d_{o2} can eventually be determined as (2) if sextant 1 is chosen as an example

$$\begin{aligned}
\cos\theta_{ia} + \cos\theta_{ib} + \cos\theta_{ic} = 0, -\frac{\cos\theta_{ib}}{\cos\theta_{ia}} - \frac{\cos\theta_{ic}}{\cos\theta_{ia}} = 1\\
d_{o1} = -\cos\theta_{ib}/\cos\theta_{ia}\\
d_{o2} = -\cos\theta_{ic}/\cos\theta_{ia}. \qquad (2)
\end{aligned}$$

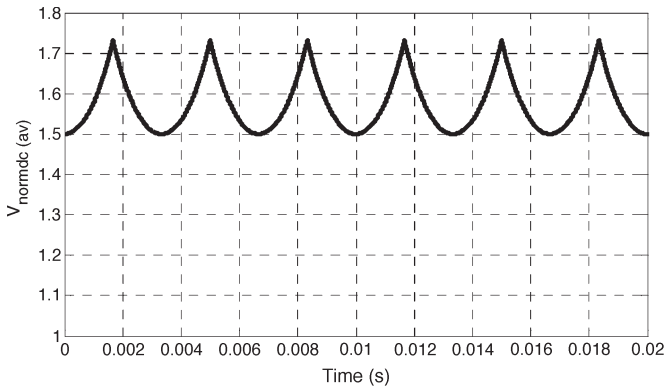

Fig. 4. Normalized dc-link voltage over a fundamental cycle when $\phi_o = 0$.

Equation (2), when multiplied by their associated output line voltages v_{ab} and v_{ac}, then leads to (3) for computing the average dc-link voltage

$$V_{\mathrm{dc(av)}} = d_{o1}v_{ab} + d_{o2}v_{ac} = \frac{3V_{om}}{2\cos\theta_{ia}} \cdot \cos\phi_o, -\frac{\pi}{6} \le \theta_{ia} \le \frac{\pi}{6}. \tag{3}$$

The same calculations can be applied to the other five sextants with the final generalized equations determined as

$$\begin{aligned} V_{\mathrm{dc(av)}} &= \frac{3V_{om}}{2|m_{\max}|}\cdot\cos\phi_o, \text{ for positive rail clamping} \\ V_{\mathrm{dc(av)}} &= \frac{3V_{om}}{2|m_{\min}|}\cdot\cos\phi_o, \text{ for negative rail clamping} \end{aligned} \tag{4}$$

where $m_{\max} = \max(m_a, m_b, m_c)$ and $m_{\min} = \min(m_a, m_b, m_c)$. The dc-link voltage is therefore a time-varying waveform with its normalized variation $V_{\mathrm{normdc(av)}}$ shown in Fig. 4 for a fundamental period and unity output power factor ($\phi_o = 0$). The observed sixth-order ripple in the dc-link voltage must obviously be compensated if the NVSC is to draw linear dc and sinusoidal ac input currents. More details about the NVSC modulation will be discussed shortly.

C. Modulation of NVSC

As mentioned in Section II-A, the NVSC requires an ac modulating reference v_{rA} and a dc reference v_{rR} for its upper and lower terminals, respectively. Both references share a common triangular carrier v_{tri} with v_{rA} always placed above v_{rR} ($v_{rA} \ge v_{rR}$). The eventual arrangement is shown in Fig. 5, where a triangular carrier with variable slope can clearly be seen. The variation of slope is necessary here to account for the different dc-link voltages applied across the NVSC when in different CSI states. The slope must therefore be adjusted according to the state durations, which, in theory, are proportional to the two active duty ratios shown in (2) when in sextant 1. More details about the carrier generation and coordination between the CSI and NVSC will be presented shortly after understanding NVSC modulation with more depth.

It should also be mentioned that, although carrier-based modulation is explicitly focused here, it is not the only possible realization technique. Space-vector method can be tried too since carrier-based and space-vector theories have long been

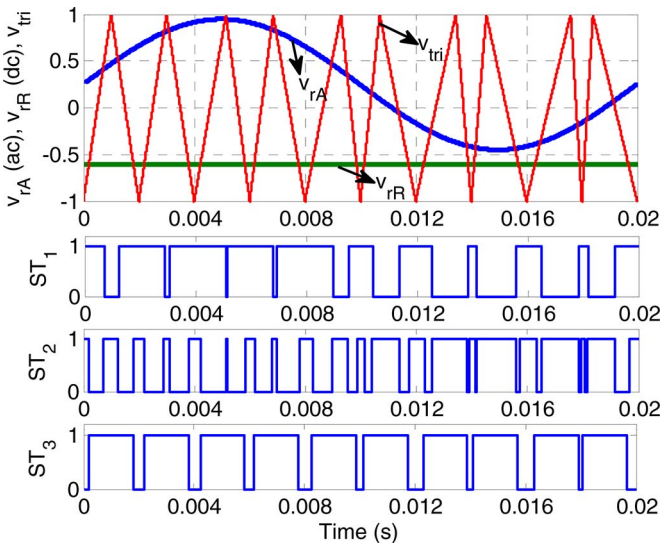

Fig. 5. Carrier-based PWM signal generation for one phase-leg of the NVSC.

proven to be equivalent. They differ mainly by their styles of implementation [22], [31]–[34], whose preferences among readers might, at times, be subjective. It is therefore not the intention here to promote any of them but to explain with the method that can better show the modulating coordination among the many input and output terminals. With that purpose defined, carrier-based approach is preferred since it shows the coordination pictorially rather than the more mathematical focus of the space-vector method.

Taking the first phase-leg of the NVSC as an example, pulsewidth-modulation (PWM) signal ST_1 (ST_3) is clearly generated by comparing the upper ac (lower dc) reference with the triangular carrier. PWM signal ST_2, on the other hand, is generated logically by XOR-ing ST_1 and ST_3. Their summarized relationships can therefore be expressed as [29], [30]

$$\begin{aligned} ST_1 &= \begin{cases} 1, & v_{rA} \ge v_{\mathrm{tri}} \\ 0, & v_{rA} < v_{\mathrm{tri}} \end{cases}, ST_3 = \begin{cases} 1, & v_{rR} \le v_{\mathrm{tri}} \\ 0, & v_{rR} > v_{\mathrm{tri}} \end{cases} \\ ST_2 &= ST_1 \oplus ST_3. \end{aligned} \tag{5}$$

Applying (5), Fig. 6 shows the zoomed-in PWM generation process for the first phase-leg in a switching period.

Parameters d_1 and d_3 marked in the figure are duty ratios obtained for switches ST_1 and ST_3 with d_3 always wider than $(1 - d_1)$ since $v_{rA} \ge v_{rR}$. The three switching states obtained at the bottom of Fig. 6 are thus in accordance with those three permitted in Table I. Despite producing the right switching states, the modulation process described so far does not guarantee linear dc and sinusoidal ac input currents. The currents will instead be distorted by the sixth-order ripple detected in the dc-link voltage. To compensate for the ripple, the ac modulating references must be normalized according to (6), whose variation term $V_{\mathrm{normdc(av)}}$ in the denominator will effectively cancel out the ripple

$$v_{rA} = \frac{v_{mA} + V_{\mathrm{off}}}{V_{\mathrm{normdc(av)}}/2} + V_{\mathrm{offup}}$$

$$v_{rB} = \frac{v_{mB} + V_{\mathrm{off}}}{V_{\mathrm{normdc(av)}}/2} + V_{\mathrm{offup}}$$

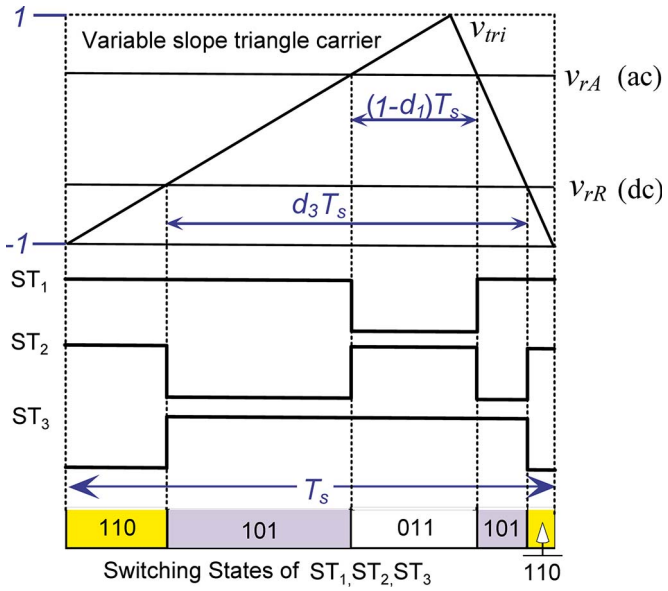

Fig. 6. PWM signal generation for one phase-leg of the NVSC in a switching period.

$$
\begin{aligned}
v_{rC} &= \frac{v_{mC} + V_{\text{off}}}{V_{\text{normdc(av)}}/2} + V_{\text{offup}} \\
v_{mA} &= m_i \cdot \cos(\omega_i t + \theta_A) \\
v_{mB} &= m_i \cdot \cos(\omega_i t + \theta_B) \\
v_{mC} &= m_i \cdot \cos(\omega_i t + \theta_C) \\
V_{\text{off}} &= -0.5\,(\max(v_{mA}, v_{mB}, v_{mC}) \\
&\quad + \min(v_{mA}, v_{mB}, v_{mC}))
\end{aligned} \tag{6}
$$

where m_i, ω_i, and θ_x ($x = A$, B, or C) are the modulation index, angular frequency, and phase angle of each input source voltage, respectively. Offset parameters V_{off} and V_{offup} are also included in (6) to represent triplen offset commonly added to raise the modulation index by 15% [28] and to lift the ac reference above its dc counterpart. These offsets, being added to phases b and c too, will cancel when detecting the sinusoidal line voltages.

The lower dc modulating reference for each phase-leg of the NVSC must also be compensated in order to produce linear input current with no distortion. The desired dc reference can, in fact, be obtained by noting that the average value of voltage v_R in Fig. 2 must contain only dc quantity in a switching period. The first step is hence to write down an expression for v_R, as shown as follows:

$$v_r = (1 - d_3) \cdot v_{\text{dc(av)}}. \tag{7}$$

If the carrier amplitude in Fig. 6 is set to vary between -1 and 1, duty ratio d_3 for ST_3 can be derived from similar-triangle theory before substituting into (7) to obtain (8) for v_R

$$
\begin{aligned}
d_3 &= \frac{1 - v_{rR}}{2} \\
v_R &= (1 - d_3) \cdot V_{\text{dc(av)}} = \frac{(1 + v_{rR})}{2} \cdot V_{\text{dc(av)}}.
\end{aligned} \tag{8}
$$

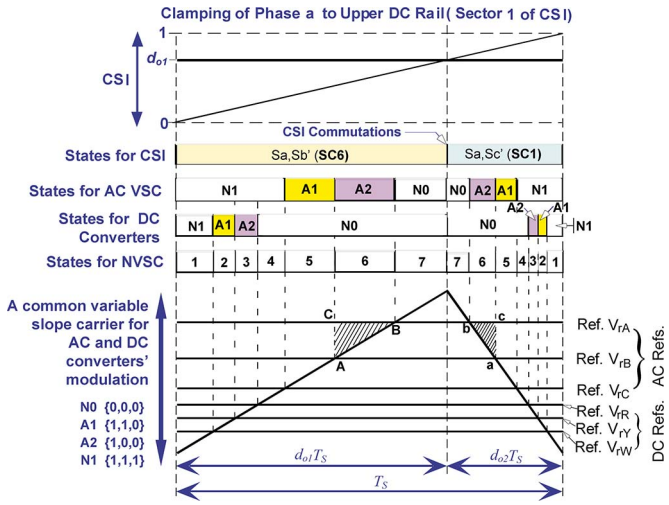

Fig. 7. Reference-carrier arrangement and state sequence for the proposed VMC.

To force v_R as a dc quantity with no low-order harmonics, the term $(1 + v_{rR})/2$ in (8) must be equalized to the right-hand term in

$$\frac{1 + v_{rR}}{2} = \frac{m_R}{V_{\text{normdc(av)}}} \tag{9}$$

where m_R is a dc quantity obtained from the higher level dc control scheme discussed in Section IV. The demanded dc modulating reference v_{rR} can eventually be deduced as (10)

$$v_{rR} = \frac{m_R}{V_{\text{normdc(av)}}/2} - 1. \tag{10}$$

D. Coordination Between CSI and NVSC

To further ensure sinusoidal output currents for the VMC, the NVSC and CSI modulations must be synchronized such that each NVSC state is divided proportionally between the two CSI state durations according to the ratio of $d_{o1} : d_{o2}$ in (2). To illustrate, the arrangement of all six modulating references and their produced state sequences are shown in Fig. 7. It can clearly be seen there that each triangular rising or falling edge spans a complete CSI state duration before the desired NVSC state division can be realized. To further double the switching frequency of NVSC while keeping the same CSI switching frequency, each rising or falling edge of the NVSC triangle carrier can be replaced by a full symmetrical triangle. Accompanying this realization is the same proportional division of the dc-link current I_{dc} between the two CSI states. Taking sextant 1 in Fig. 3 as an example, currents flowing through phases b and c of the CSI can then be related by $i_b/i_c = d_{o1}/d_{o2}$, which would give rise to sinusoidal output currents if I_{dc} contains a $\cos\theta_{ia}$ term. Mathematical proof for this can be found in the next section.

In the meantime, it should be pointed out that switching states N0, A1, A2, and N1 of the upper three ac terminals or lower three dc terminals of the NVSC in Fig. 7 assume the same state notations as the traditional six-switch dc/ac inverter. For instance, state A1{1,1,0} of the upper three ac

terminals means upper switches $ST_1 = \text{ON}$, $ST_4 = \text{ON}$, and $ST_7 = \text{OFF}$. Similarly, state A1 of the lower three dc terminals means lower switches $ST_3 = \text{OFF}$, $ST_6 = \text{OFF}$, and $ST_9 = \text{ON}$. These signals can then be XOR-ed in (5) to get statuses for the middle three switches ST_2, ST_5, and ST_8. Combining the upper and lower intermediate states then results in seven overall NVSC states. Each NVSC state contains on and off information of all the nine switches. For example, state 6 is obtained by combining the upper A2{1,0,0} and lower N0{0,0,0} intermediate states. Its first number "1" in A2 then means $ST_1 = 1$, and its first number "0" in N0 means $ST_3 = 1$. Together, they give $ST_2 = (ST_1)XOR(ST_3) = 0$.

Like their intermediate states, all seven NVSC states are divided proportionally between the two CSI state durations according to the ratio of $d_{o1} : d_{o2}$. To illustrate, the shadowed triangles ΔABC and Δabc in Fig. 7 are referred to, where state 6 is shown to be correctly divided since $BC/bc = d_{o1}/d_{o2}$. Proportional division through synchronizing the NVSC triangular carrier with the CSI states also has another advantage illustrated by Fig. 7. It can be seen there that CSI commutations occur only within NVSC states 1 and 7. Within these two states, no dc-link current flows, and hence, no switching losses are generated by the CSI commutations.

III. Mathematical Proof for Sinusoidal Output Currents

Sinusoidal input and output currents are basic requirements defined for most traditional ac/ac matrix converters. The same applies to the proposed VMC but with more difficulties involved since it also draws linear undistorted currents from the dc sources. Its mathematical proof is therefore slightly more complex and is hence discussed here. For the inputs, it has already been mentioned in Section II-C that sinusoidal ac and linear dc currents will be drawn if their references are normalized according to (6) and (10). It is therefore the intention now to prove sinusoidal output currents for the CSI, whose first step is to find the average dc-link current $I_{\mathrm{dc(av)}}$ per switching period. For that, it is noted from Fig. 2 that $I_{\mathrm{dc(av)}}$ can be written as

$$I_{\mathrm{dc(av)}} = i_1 + i_2 + i_3 \tag{11}$$

where the individual average phase-leg currents i_1, i_2, and i_3 can be determined from the switching states shown in Fig. 6 and the equivalent circuits shown in Fig. 8 for a NVSC phase-leg.

To illustrate, i_1 in Fig. 2 is considered, whose value can be $i_A + I_R, i_A$ or zero depending on whether ST_1, ST_2, and ST_3 are switched to {110}, {101}, or {011}. Here, i_A and I_R are the input ac and dc currents of the leftmost phase-leg, respectively. Noting further from Fig. 6 that the time durations for states {110} and {101} are $(1 - d_3)T_S$ and $(d_1 + d_3 - 1)T_S$, respectively, i_1 can eventually be averaged as

$$\begin{aligned} i_1 &= (1 - d_3) \cdot (i_A + i_R) + (d_1 + d_3 - 1) \cdot i_A \\ &= (1 - d_3) \cdot i_R + d_1 \cdot i_A. \end{aligned} \tag{12}$$

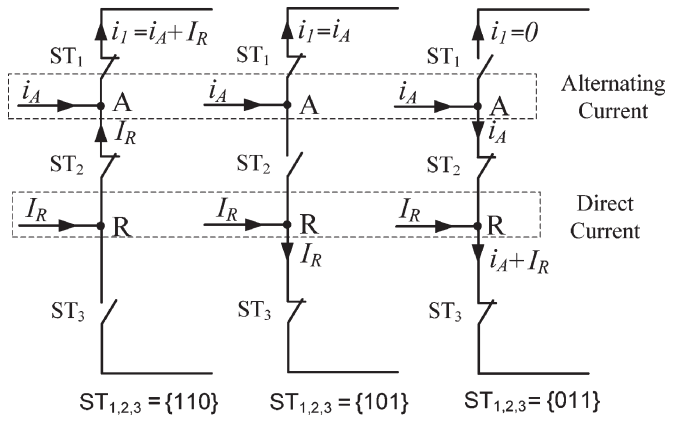

Fig. 8. Equivalent circuits of a NVSC phase-leg.

Currents i_2 and i_3 can similarly be averaged before substituting into (11) to find $I_{\mathrm{dc(av)}}$ as

$$\begin{aligned} I_{\mathrm{dc(av)}} &= d_1 \cdot i_A + d_4 \cdot i_B + d_7 \cdot i_C \\ &\quad + (1 - d_3) \cdot I_R + (1 - d_6) \cdot I_Y + (1 - d_9) \cdot I_W \end{aligned} \tag{13}$$

where i_B, i_C, I_Y, and I_W are the remaining ac and dc input currents. An example expression for the ac input current can further be written as

$$i_A = I_i \cdot \cos(\omega_i t + \theta_A + \varphi_i) \tag{14}$$

where I_i and φ_i represent the amplitude and power factor angle of the input current. Expressions for i_B and i_C have the same form except those phase-shifted by $-2\pi/3$ and $2\pi/3$, respectively.

Duty ratios d_1 and d_3 can also be determined by applying similar-triangle theory to Fig. 6, where an expression for d_3 has already been derived in (8). Expression for d_1 (and, in fact, d_4, d_7, d_6, and d_9) can similarly be derived as

$$\frac{(1 - d_1) \cdot T_s}{T_s} = \frac{1 - v_{rA}}{2} \Rightarrow d_1 = \frac{1 + v_{rA}}{2}. \tag{15}$$

Substituting (6), (8), (14), and (15) into (13) then leads to another intermediate expression for $I_{\mathrm{dc(av)}}$ written as follows:

$$I_{\mathrm{dc(av)}} = \frac{\frac{3}{2} m_i \cdot I_i \cdot \cos\varphi_i + m_R \cdot I_R + m_Y \cdot I_Y + m_W \cdot I_W}{V_{\mathrm{normdc(av)}}}. \tag{16}$$

Taking sextant 1 of the CSI ($-\pi/6 \le \theta_{ia} \le \pi/6$) as an example, $V_{\mathrm{normdc(av)}}$ is deduced from $V_{\mathrm{dc(av)}}$ in (3) after setting $V_{om} = 1$. Substituting it into (16) eventually gives the final expression for $I_{\mathrm{dc(av)}}$ as

$$\begin{aligned} I_{\mathrm{dc(av)}} = \Bigg(& m_i \cdot I_i \cdot \cos\varphi_i + \frac{2}{3} \cdot m_R \cdot I_R \\ & + \frac{2}{3} \cdot m_Y \cdot I_Y + \frac{2}{3} \cdot m_W \cdot I_W \Bigg) \cdot \cos\theta_{ia} / \cos\phi_o. \end{aligned} \tag{17}$$

With $I_{\mathrm{dc(av)}}$ determined and sextant 1 considered as an example, the three-phase output currents of the CSI can be

computed as (18) after substituting in expressions for d_{o1} and d_{o2} from (2)

$$\begin{aligned} i_a &= I_{\mathrm{dc(av)}} = I_{\mathrm{out}} \cdot \cos\theta_{ia} \\ i_b &= -I_{\mathrm{dc(av)}} \cdot d_{o1} = I_{\mathrm{out}} \cdot \cos\theta_{ib} \\ i_c &= -I_{\mathrm{dc(av)}} \cdot d_{o2} = I_{\mathrm{out}} \cdot \cos\theta_{ic} \\ I_{\mathrm{out}} &= \left(m_i \cdot I_i \cdot \cos\varphi_i + \frac{2}{3} \cdot m_R \cdot I_R \right. \\ &\quad \left. + \frac{2}{3} \cdot m_Y \cdot I_Y + \frac{2}{3} \cdot m_W \cdot I_W \right) \cos\phi_o. \end{aligned} \quad (18)$$

Expression (18) obviously represents the intended three-phase sinusoidal output currents being produced by the VMC. It should, however, be noted that the one mentioned earlier is only one out of a few possible ways of derivation. One alternative is to consider the power balance theory, from which $I_{\mathrm{dc(av)}}$ in (17) can also be derived. The theory states that, with sinusoidal ac and linear dc input currents guaranteed by (6) and (10), total instantaneous input power P will be a constant. That further means that instantaneous dc-link power and three-phase output power will be constant too and equal to P due to the absence of passive component within the VMC. The dc-link current $I_{\mathrm{dc(av)}}$ would hence vary inversely with the dc-link voltage $V_{\mathrm{dc(av)}}$, which, when applied to sextant 1, leads to the following similar expression for $I_{\mathrm{dc(av)}}$:

$$\begin{aligned} V_{\mathrm{dc(av)}} \cdot I_{\mathrm{dc(av)}} &= P \\ I_{\mathrm{dc(av)}} &= I_{\mathrm{out}} \cdot \cos\theta_{ia} \\ I_{\mathrm{out}} &= \frac{2P}{3V_{om} \cdot \cos\phi_o}. \end{aligned} \quad (19)$$

IV. Control Algorithms

The earlier described modulation schemes are based on (6) and (10), which require some intermediate references v_{mA}, v_{mB}, v_{mC}, and m_R for processing. These references are generated by the higher level control schemes whose purpose is to ensure accurate power dispatches from the sources. Their details are described now mainly for the NVSC since no control scheme is needed by the output CSI whose purpose is mainly to invert the fictitious dc-link current to a set of three-phase output currents.

A. Control of Upper NVSC AC Terminals

Unlike the usual twelve-switch ac/dc/ac converter, the VMC does not have a dc-link capacitor and hence does not require any dc-link voltage regulation. Its input and output powers are also equal, and hence, it does not need to be controlled separately. Reactive power regulation wise can still be separated between the ac input side and output grid side. For the input side, its reactive current command is usually set to zero for unity power factor generation. The same can be done for the output grid side, if desired, by shifting the output power factor angle ϕ_o in (1)

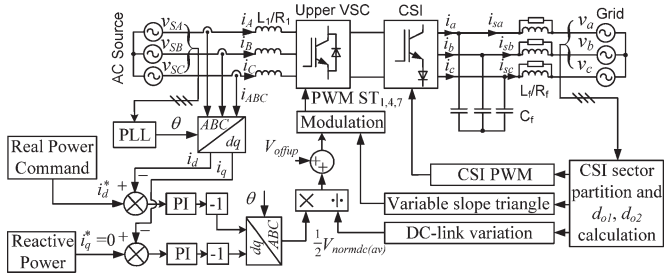

Fig. 9. Block diagram for ac source control.

to zero. For nonunity output power factor, ϕ_o can vary within the range of $-\pi/6$ to $\pi/6$ but should not be excessive since it leads to a lower dc-link voltage according to (4). Varying of ϕ_o is, however, not further discussed here though, because it is a modulation process that has no impact on the control schemes.

Referring back to Fig. 2, voltage–current relationships for the ac input can undoubtedly be written as (20) and (21) in the ABC and d–q coordinate frames, respectively

$$L_1 \frac{d}{dt} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} + R_1 \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} v_{SA} \\ v_{SB} \\ v_{SC} \end{bmatrix} - \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \quad (20)$$

$$L_1 \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R_1 & \omega_i L_1 \\ -\omega_i L_1 & -R_1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} - \begin{bmatrix} v_d \\ v_q \end{bmatrix}. \quad (21)$$

These equations are similar to those of a standard rectifier, which means that earlier proportional–integral (PI) control in the synchronous d–q frame can also be used with the VMC. The recommended control scheme for the ac input is therefore shown in Fig. 9, where the ac input voltages v_{SA}, v_{SB}, and v_{SC} are sensed to provide phase angle information needed for d–q transformation. Two PI controllers, whose parameter tuning is based on [36], are then used for regulating the measured d–q currents i_d and i_q accordingly. For i_d, its command i_d^* is decided by a maximum powerpoint tracker (MPPT) or power dispatch order according to $i_d^* = P^*/|v_S|$, where P^* and $|v_S|$ are the active power command and ac source voltage amplitude, respectively. Current i_q, on the other hand, has its command i_q^* set to zero for unity input power factor assuming that the d-axis has been properly aligned to the grid voltage vector. The resulting PI control outputs are then converted back to the stationary ABC frame to give the intermediate references of v_{mA}, v_{mB}, and v_{mC}. These intermediate signals are needed by (6) to produce the final modulating references for channeling to the NVSC modulation block. Details of the modulation block have already been discussed in Section II-C.

B. Control of Lower NVSC DC Terminals

Control of the lower NVSC dc terminals is comparably simpler since it does not require grid synchronization and reactive power consideration. Only active power from each dc source needs to be controlled, which, in concept, is similar to that

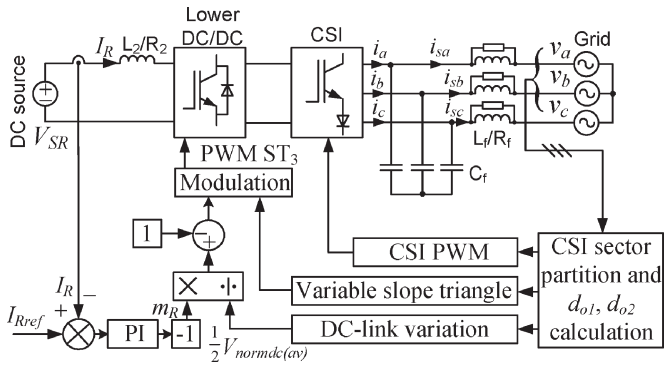

Fig. 10. Block diagram for dc source control.

found with a normal dc/dc converter since they share the same terminal relationship spelled in (22)

$$V_{SR} - v_R = L_2 \cdot dI_R/dt + R_2 \cdot I_R. \tag{22}$$

Control of each NVSC dc terminal can hence be realized with a simple PI controller in the stationary frame. Control block diagram of the scheme can be found in Fig. 10, where current reference $I_{R\text{ref}}$ can be seen tracked by the measured input current I_R through a PI controller. Per the ac controller, current reference $I_{R\text{ref}}$ is obtained from an MPPT or power dispatch command, which, according to the notation used in Fig. 10, can be expressed as $I_{R\text{ref}} = P^*_{\text{dc}}/V_{SR}$, where P^*_{dc} is the active power command. Output from the PI controller is then the demanded intermediate reference m_R to be processed by (10) before generating the required gating signals through the earlier mentioned carrier-based modulation.

C. Potential Applications

With the aforementioned power control schemes, the proposed VMC with ac and dc input terminals can be used with a wind energy generator and multiple energy storage systems with either high energy or power density. An example combination can be a direct-drive permanent magnet synchronous generator (PMSG) tied with hybrid battery/ultracapacitor energy storages. The input current command from the PMSG can be obtained from an MPPT, whose value might fluctuate because of the changing wind speed. The hybrid storages can therefore operate like dispatchable sources, whose responsibility is to alleviate the power fluctuation. Where desired, the wind generator can also be replaced by an ac-type low-speed flywheel to create a strong hybrid storage system, whose individual characteristics should preferably complement each other.

V. Simulation and Experimental Results

To validate the proposed grid application of the VMC, the system shown in Fig. 2 was first simulated in Matlab/Simulink using the PLECS power electronic libraries, before building a laboratory prototype for hardware verification. Parameters used for the simulation and experiment were the same with the grid parameters set to 50 Hz/100 V (phase rms). The three-phase ac input source and single dc source, on the other hand, were set to 40 Hz/50 V (phase rms) and 55 V, respectively. Only one dc

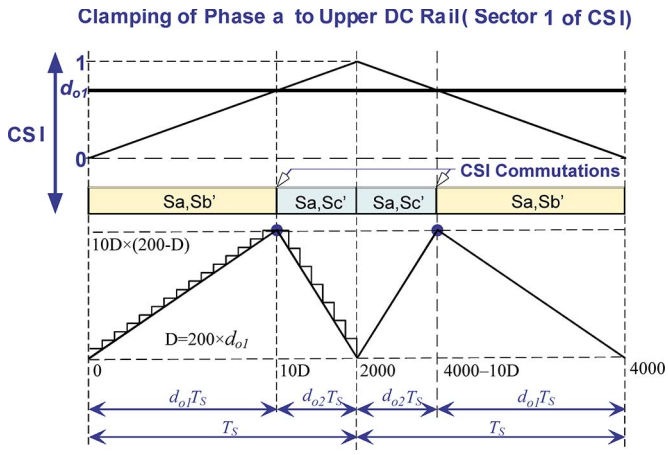

Fig. 11. FPGA realization of the triangular carrier.

source connected to terminal R of Fig. 2(b) was used here because of hardware limitation in the laboratory. This limitation, to no extent, would affect findings discussed in this paper. Other parameters used were summarized as $L_1/R_1 = 6.3$ mH/0.3 Ω, $L_2/R_2 = 10$ mH/0.3 Ω, $L_f/R_f = 3$ mH/0.2 Ω, and $C_f = 40$ μF, respectively. A 20-Ω resistor R_d was also connected in parallel with L_f for damping purposes like in most matrix converters. The value of R_d should not be too low since it will worsen the filtering effect even though damping will be improved.

For the experimental system, the discussed modulation and control schemes can be implemented with a dSPACE controller and a Xilinx field-programmable gate array (FPGA). The former was used to realize the CSI sector partition and closed-loop control schemes discussed in Section IV. Slope information (duty ratios of CSI) for a 10-kHz triangular carrier and three-phase ac and dc modulating references was then transmitted to the FPGA for gating signal generation for the NVSC. The FPGA also generated a synthesized PWM signal based on the duty ratios of CSI and transmitted to dSPACE controller, which would then produce six-channel CSI gating signals using the six-sector information as discussed in Section II-B. Particularly, for the variable-slope triangular carrier, it was implemented in the FPGA with a defined variable D, whose meaning was given as follows:

$$D = \begin{cases} 200 \times d_{o1} & \text{if } d_{o1} > d_{o2} \\ 200 \times d_{o2} & \text{if } d_{o2} > d_{o1}. \end{cases} \tag{23}$$

A scaling factor of 200 was purposely introduced to (23) to convert the fractional duty ratio into an integer that was more suitable for FPGA manipulation. Theoretical range of variation for D could therefore be expressed as $100 \leq D \leq 200$, where the maximum of 200 was usually lowered slightly (e.g., 190) to avoid producing overly steep slope. In the FPGA, the input clock frequency was 100 MHz, which, when divided, gave a 20-MHz clock for the triangular carrier generation. A counter was also defined based on the 20-MHz clock, which would then count up to 2000 in a 10-kHz carrier period. Its maximum was set to 4000, which, as shown in Fig. 11, corresponded to two switching periods. The amplitude of the carrier was set as $10D \times (200 - D)$, which, needless to say, was time

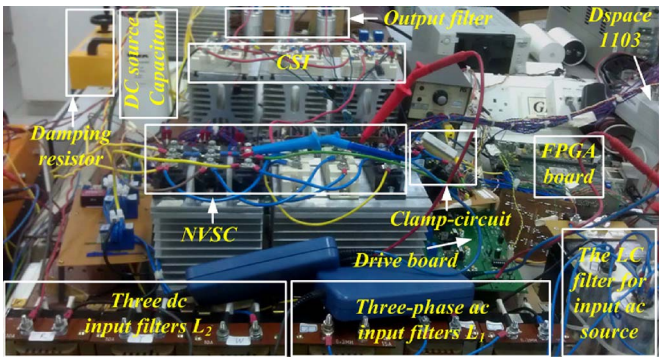

Fig. 12. Hardware experimental system.

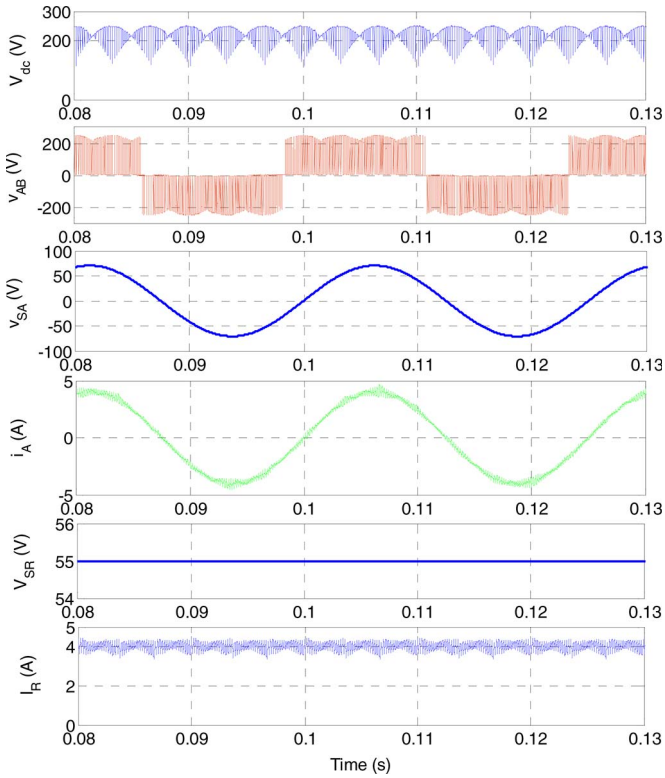

Fig. 13. Simulated dc-link voltage, ac unfiltered input line voltage, ac source phase voltage/current, and dc source voltage/current.

varying at different D's. The purpose here was to guarantee that the incremental and decremental counting steps for the rising and falling slopes were integers. This was indeed the case as understood from Fig. 11, where the incremental step was $(200 - D)$ and the decremental step was D. Since the carrier amplitude was time varying, the last step was to scale the NVSC modulating references accordingly before performing the comparison. With the modulator and controller realized and placed besides the converter, Fig. 12 shows the eventual hardware prototype built.

A. Simulation Results

Figs. 13 and 14 show the simulated waveforms with ideal switches studied when the input ac and dc reference currents were set to 4 A. The ac and dc powers fed to the VMC were then 424 and 220 W, respectively. The output grid current amplitude

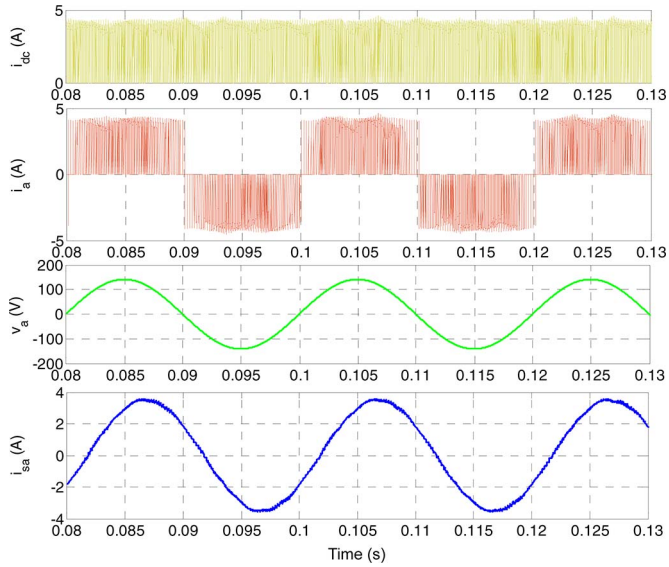

Fig. 14. Simulated dc-link current, ac unfiltered output current, grid phase voltage, and filtered grid current.

was read as 3.5 A, and the phase angle difference between grid voltage and current was read as 32.4°. The real power injected into grid was calculated to be about 626 W. The dc-link voltage was also noted to have a sixth-order variation formed by the different ac grid line voltages. This variation did not distort the ac input and output current waveforms, whose total harmonic distortions (THDs) were computed as 4.31% for input i_A and 1.93% for output i_{sa}.

Power level of the system was next raised to about 10 kW for demonstrating its dynamic response. The input ac and dc source voltages were both raised to 120 V (phase rms for ac) with all three dc sources now connected to the lower NVSC terminals. The grid voltage was also raised to 240 V (phase rms), accompanied by an increase in filter capacitance C_f from 40 to 50 μF for better switching current suppression. Other than these, all other parameters were kept unchanged. Simulation was then repeated with Fig. 15 plotting the obtained results. Clearly, before $t = 0.1$ s, there was no power flow from the ac source, and the three dc source currents were set to 30 A. After $t = 0.1$ s, the ac source current was raised to 40 A, while the dc sources were turned off.

Other results were plotted in Fig. 16, where the dc-link current peak was shown to change from 90 to 40 A at $t = 0.1$ s. The earlier 90 A was contributed by the summation of all three 30-A input dc currents when the top three $(ST_1, ST_4,$ and $ST_7)$ and middle $(ST_2, ST_5,$ and $ST_8)$ three switches were turned on. The later 40 A was instead contributed by the three-phase 40-A input ac currents, whose peaks were phase-shifted by 120°, and hence did not triple at the dc link. This current peak transition was also observed with the unfiltered grid current i_a, obtained directly from the dc-link current (see the second trace in Fig. 16). Harmonic content of i_a was thus higher before $t = 0.1$ s because of its higher current peak. This higher harmonic content was further transferred to the filtered grid current i_{sa}, whose THD was then expected to be higher before $t = 0.1$ s. This was confirmed in simulation, where THD values for i_{sa} before and after transient were read as 4.11% and 2.15%,

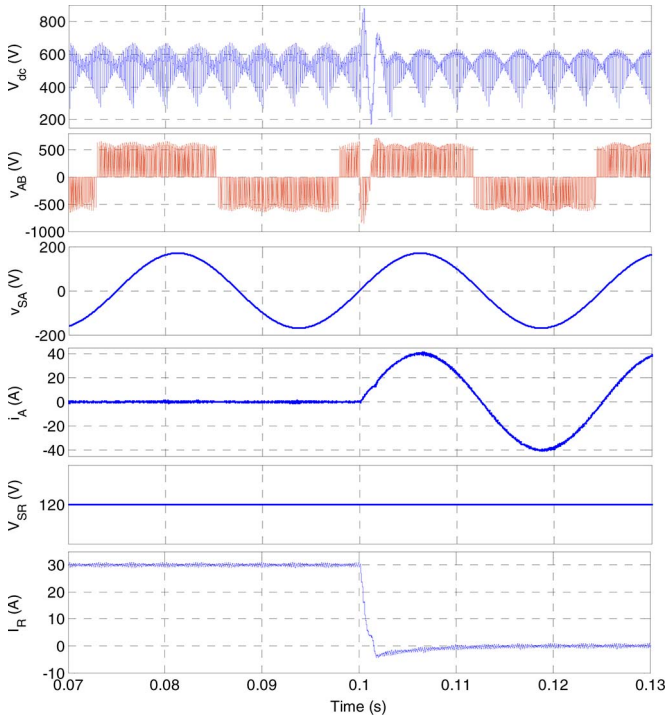

Fig. 15. Simulated dc-link voltage, ac unfiltered input line voltage, ac source phase voltage/current, and dc source voltage/current when subjected to dynamic source reference current changes.

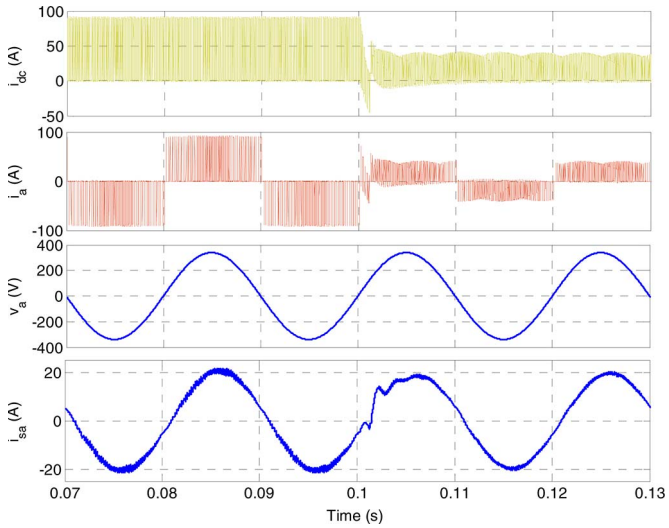

Fig. 16. Simulated dc-link current, ac unfiltered output current, grid phase voltage, and filtered grid current when subjected to dynamic source reference current changes.

respectively, even though the filtered fundamental component remained nearly constant throughout the illustrated duration (see the last trace in Fig. 16).

The simulated system was next modified with some resistances added to represent practical semiconductor losses. The purpose was to compare losses produced by the NVSC and its equivalent twelve-switch converter (six parallel two-switch phase-legs). Input and output conditions for the two cases were kept the same with their ac and dc current references set at 4 A. The obtained efficiencies were 92% with the NVSC and

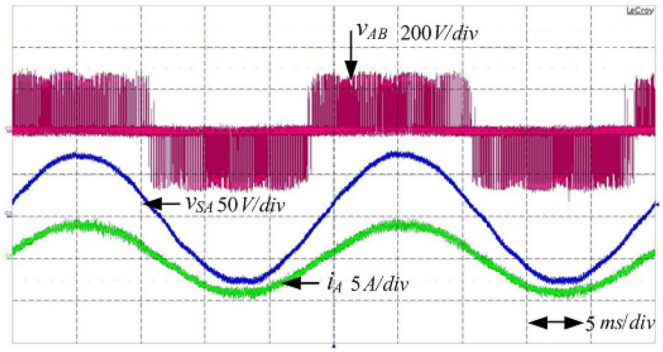

Fig. 17. Measured unfiltered line voltage, phase voltage, and phase current of ac input source.

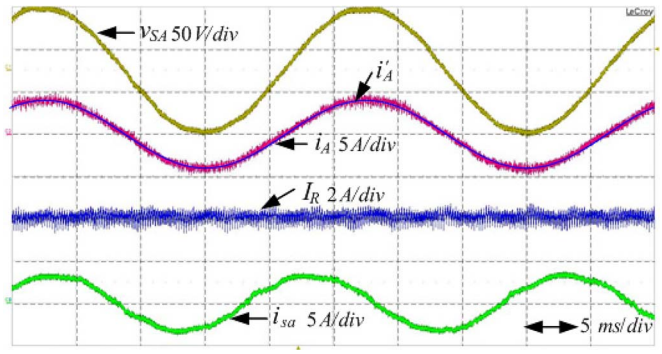

Fig. 18. Measured ac source phase voltage/current, dc source current, and grid current.

90% with the twelve-switch converter. These numbers were close, meaning that using the NVSC would not result in higher semiconductor losses for the VMC. This was unlike the application in [29] where the dc-link voltage had to be doubled. The dc-link voltages endured here by the NVSC and twelve-switch converter for the VMC were the same and, in fact, fixed by the grid and CSI. Voltage stresses and semiconductor losses were therefore not expected to rise. Instantaneous currents flowing through the upper ST_1 and lower ST_3 switches of the NVSC might, however, be of concern since they are expressed as $i_A + I_R$ when in state $ST_{1,2,3} = \{110\}$ and $\{011\}$, respectively. During the positive cycle of i_A, $i_A + I_R$ is increased, while during its negative cycle, $i_A + I_R$ is decreased.

B. Experimental Results

Fig. 17 shows waveforms obtained at the ac input side, which were undeniably close to those simulated in Fig. 13. Fig. 18 shows more measured input and output current waveforms, whose 4-A input ac and dc current references were tracked correctly (i'_A in the figure represents ac input current reference). The measured ac input power factor was also read as close to unity, which was indeed the value set for the experiment. The only shortfall here was the poorer current waveform quality, which was probably due to the digitization of the variable-slope carrier. The impact of the digitization was expected to be more serious at the six sextant crossover boundaries, during which one of the slopes became much steeper according to Fig. 12.

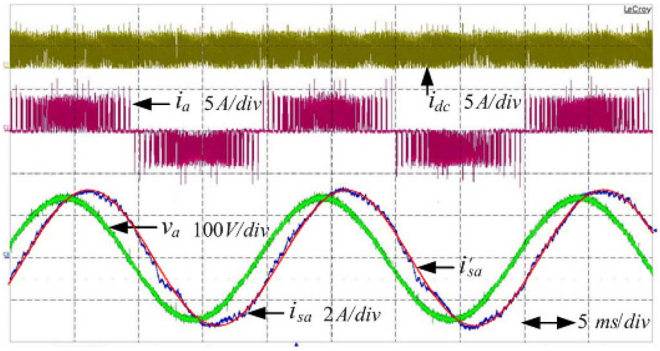

Fig. 19. Measured dc-link current, unfiltered output current, grid phase voltage, and filtered grid current.

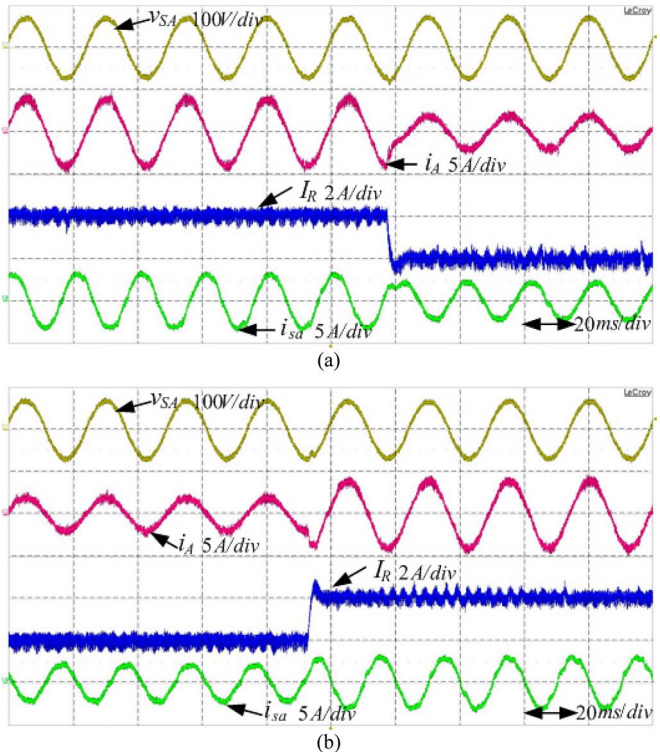

Fig. 20. Dynamic responses of ac/dc input currents and grid current during power (a) decrease and (b) increase transients.

The affected slope then had to be capped at a maximum value throughout the duration of sextant commutation. The capped value would, no doubt, introduce errors to the waveform of grid currents. The error magnitude would depend on the maximum carrier slope permitted. In general, the higher the carrier slope limit, the smaller would be the errors.

Fig. 19 continues to show more waveforms measured at the ac output end, whose filtered grid current peak was read as approximately 3.35 A. This value was slightly smaller than the simulated value of 3.5 A obtained with ideal switches. The unfiltered current i_a was also observed to be in phase with the grid voltage v_a, representing unity output power factor. With i_a and v_a in phase, the filtered grid current i_{sa} (and its reference i'_{sa}) must lag v_a since it was obtained by subtracting the filter capacitor current from i_a. Noting too that this filter capacitor current was a constant under the same grid voltage condition, its influence was expected to be smaller for bigger i_a and i_{sa}. To next test the system dynamic response, the input source current references were changed. Fig. 20(a) and (b) shows the input and output current waveforms obtained when the ac and dc input current references dropped from 4 to 2 A and then back to 4 A. Regardless of the changes, accurate current and power factor tracking was maintained with no prominent deterioration observed with any of the waveforms.

VI. Conclusion

A VMC capable of integrating hybrid ac/dc input sources to the grid has been proposed in this paper. Comparing with the IMC, the proposed converter uses a unique nine-switch front end for connecting a three-phase ac and three dc sources to the grid. It operates in the reverse-boost mode, which is more suitable for modern alternative sources whose voltages are usually lower than that of the grid. Proper modulation and control schemes have also been developed, whose realization helps to ensure accurate power dispatches and near-sinusoidal input and output currents. Mathematical derivation, simulation, and experimental results have already validated the findings presented.

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