A Simple Test Structure for Directly Extracting Substrate Network Components in Deep n-Well RF-CMOS Modeling

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***Abstract*—A simple test structure is proposed for accurately extracting the substrate network parameters of a radio-frequency MOSFET with deep n-well implantation from two-port measurements. The test structure with the source, drain, and gate terminals all connected together is used as port one, while the bulk terminal as port two, making the substrate network distinctly accessible in measurements. A methodology is developed to directly extract the parameters for the substrate network from the measured data. The method is further verified by the excellent match between the measured and simulated output admittances on the extracted parameters for a 16-finger nMOSFET of common-source configuration operated in different bias conditions.**

***Index Terms*—Deep n-well (DNW), parameter extraction, radio-frequency (RF) MOSFET, substrate network.**

I. Introduction

ALTHOUGH many advantages of deep n-well (DNW) implantation in CMOS mixed-signal/radio-frequency (RF) circuit designs have been validated [1]–[3], a reasonable methodology for accurately extracting the substrate network parameters of DNW RF MOSFETs has not been reported. The substrate network in CMOS is of utmost importance in predicting the device output characteristics at RFs. Different from an RF MOSFET without DNW implantation, DNW actually partitions the substrate of a DNW RF MOSFET into three parts: the DNW itself, p-well in the DNW, and the original substrate where the DNW is formed. Since the coupling between DNW and p-well, as well as between DNW and the original substrate, exists no matter what the electrical configuration is, conventional substrate networks and the corresponding extraction methods become too simple to accurately extract the substrate network parameters of DNW RF MOSFETs.

Most test structures used in measuring the substrate characteristics of RF MOSFETs have a two-port configuration with the gate terminal served as port one, the drain terminal defining port two, and the source shorted to the p-substrate serving as the common terminal [4]–[7]. This configuration fails to capture the interaction between the source and bulk terminals and those between the source and the drain terminals through the bulk. Different test structures have been proposed for characterizing the distributed substrate network [8]–[11], and some have to employ three-port [9] or four-port measurement [11]. A common gate arrangement can help access the substrate from both the source and the drain side [8], whereas the gate network is also included during measurement via the gate–source and gate–drain admittances. Employing the on-probe capacitance of a ground–power–ground (GPG) probe to ac short, the extrinsic gate and bulk [10] are free of the problem in [8]. However, this approach is valid only at low frequencies, as the GPG probe provides a nonideal short at higher frequencies. Furthermore, all the test structures and measurement setups in [4]–[11] are developed for modeling RF MOSFETs without DNW implantation.

In this letter, a simple test structure is proposed to specifically target the characterization of DNW RF MOSFETs. For the first time, a novel substrate network is developed, considering DNW and the effects due to the capacitive coupling of the p-well and the nature substrate. A direct extraction scheme for network parameters is provided.

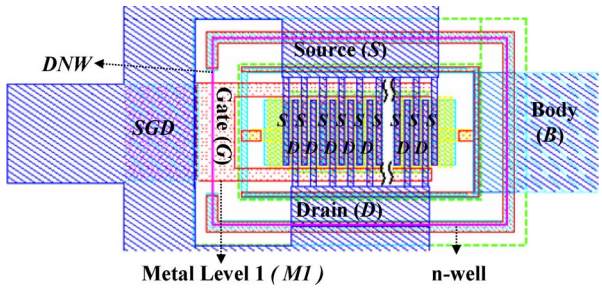

Fig. 1. Simplified layout plane figure of the proposed test structure for DNW nMOSFETs. The thickness of the DNW is approximately 0.8 μm. The conduct voltage of junction diodes ($V_{j\mathrm{th}}$) is about 0.37 V.

II. Test Structure, Equivalent Circuit, and Parameter Extraction of Substrate Network

The proposed test structure, with the source (S), drain (D), and gate (G) terminals connected together as shown in Fig. 1, makes the substrate network distinctly accessible in measurements. This enables the direct extraction of the substrate

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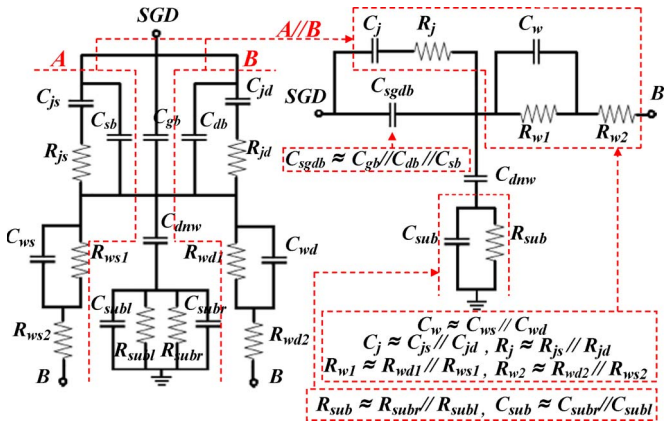

Fig. 2. Equivalent circuits of the proposed test structure. Source, drain, and gate resistances are ignored because the impedance of the series resistances is negligible compared with those of junction capacitance and p-well and p-substrate resistances. Since the topology from S to B is same as that from D to B, the (left) complete equivalent circuit can be reduced to (right) a T-network by using (low right) a simple approach and enables the direct extraction of the substrate network from the Z-parameters.

characteristics as it becomes clear in the equivalent circuit analysis, which follows later in this section. For this purpose, a set of DNW n-MOSFETs with different numbers of fingers [the N_f of each device is 1, 2, 4, 8, 16, 32, and 64; the length (L_f) and width (W_f) for each finger are fixed at 0.18 and 5 μm, respectively] was fabricated using SMIC 0.18-μm 1P6M RF-CMOS process. $M1$ is used to connect $S/D/G$ terminals together and defined as port one, while the body (B) is defined as port two for the two-port RF measurement.

Based on the substrate network shown in Fig. 4, the complete equivalent circuit of the test structure can be drawn as shown at the left of Fig. 2 and be reduced to a T-network with $S/G/D$ and B as the RF terminals. C_{js} and C_{jd} are the junction capacitances and resistances of S/D regions with the embedded p-well (within DNW). C_{sb}, C_{gb}, and C_{db} indicate the extrinsic S-to-B, D-to-B, and G-to-B capacitances. R_{js}, R_{ws1}, R_{ws2} and R_{jd}, R_{wd1}, R_{wd2} are resistances of p-well under S and D regions, respectively. $C_{\rm dnw}$ represents the capacitance caused by DNW. $R_{\rm subl}$ and $R_{\rm subr}$ are the p-substrate resistances. Four special elements C_{ws}, C_{wd}, $C_{\rm subl}$, and $C_{\rm subr}$ are introduced to capture the capacitive coupling effect in p-well and p-substrate. The T-network shown in Fig. 2 is analyzed in terms of Z-parameters with the ground terminal as reference, and the Z-parameters can be calculated approximately with the following:

$$[Z_{11}-Z_{12}]^{-1}=\frac{\omega^2C_j^2R_j}{1+\omega^2C_j^2R_j^2}+j\frac{\omega C_j}{1+\omega^2C_j^2R_j^2}+j\omega C_{\rm sgdb} \tag{1}$$

$$Z_{22}-Z_{21}=R_{w2}+\frac{R_{w1}}{1+\omega^2R_{w1}^2C_w^2}-j\omega\frac{R_{w1}^2C_w}{1+\omega^2R_{w1}^2C_w^2} \tag{2}$$

$$Z_{12}=\frac{R_{\rm sub}}{1+\omega^2R_{\rm sub}^2C_{\rm sub}^2}-j\omega\frac{R_{\rm sub}^2C_{\rm sub}}{1+\omega^2R_{\rm sub}^2C_{\rm sub}^2}-j\frac{1}{\omega C_{\rm dnw}}. \tag{3}$$

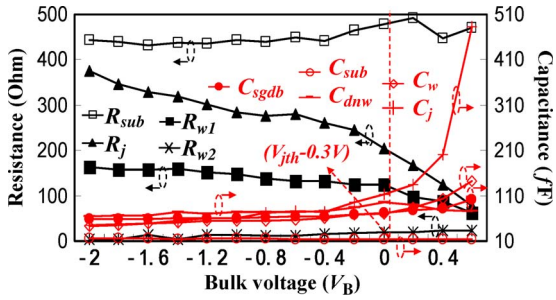

Fig. 3. Extracted substrate resistances and capacitances of the 16-finger DNW nMOSFET at different V_B's, when $V_{\rm SGD}=0$ V.

Furthermore, the real and imaginary parts of the aforementioned Z-parameter expressions can be rearranged as follows:

$$\frac{\omega^2}{\mathrm{Re}\{[Z_{11}-Z_{12}]^{-1}\}}=\omega^2R_j+\frac{1}{C_j^2R_j} \tag{4}$$

$$C_{\rm sgdb}=\omega^{-1}\left\{\mathrm{Im}\left\{[Z_{11}-Z_{12}]^{-1}\right\}-\frac{\omega C_j}{1+\omega^2C_j^2R_j^2}\right\} \tag{5}$$

$$-\frac{\omega}{\mathrm{Im}[Z_{22}-Z_{12}]}=\omega^2C_w+\frac{1}{R_{w1}^2C_w} \tag{6}$$

$$R_{w2}=\mathrm{Re}[Z_{22}-Z_{12}]-\frac{R_{w1}}{1+\omega^2R_{w1}^2C_w^2} \tag{7}$$

$$\{\mathrm{Re}[Z_{12}]\}^{-1}=R_{\rm sub}^{-1}+\omega^2R_{\rm sub}C_{\rm sub}^2 \tag{8}$$

$$C_{\rm dnw}=-\{\omega[\mathrm{Im}[Z_{12}]+\omega R_{\rm sub}^2C_{\rm sub}/(1+\omega^2R_{\rm sub}^2C_{\rm sub}^2)]\}^{-1}. \tag{9}$$

Using (4) and (6), R_j and C_w can be extracted from the slopes of the linear regression of the experimental $\omega^2/\mathrm{Re}\{[Z_{11}-Z_{12}]^{-1}\}$ versus ω^2 and $-\omega/\mathrm{Im}[Z_{22}-Z_{12}]$ versus ω^2, respectively. After subtracting R_j and C_w, (4) and (6) give C_j and R_{w1}. Furthermore, (5) and (7) give $C_{\rm sgdb}$ and R_{w2}. Using (8), $R_{\rm sub}$ and $C_{\rm sub}$ can be determined from the intercept and the linear regression of the experimental $1/\mathrm{Re}[Z_{12}]$ versus ω^2, and the slope gives $C_{\rm sub}$ after subtracting $R_{\rm sub}$. After subtracting $R_{\rm sub}$ and $C_{\rm sub}$, (9) gives $C_{\rm dnw}$. Thus, all elements of the simplified equivalent circuit of Fig. 2 are extracted.

III. Comparison of the Measured and Simulated Results

Two-port S-parameters were measured and de-embedded $(open+short)$ for parasitics introduced by GSG PAD using an Agilent E8363B network analyzer and a CASCADE Summit probe station. Then, the de-embedded S-parameters were transformed to Z-parameters for the substrate network parameter extraction.

The substrate parameters extracted from the 16-finger DNW nMOSFET test structure at various bulk biases (V_B) are shown in Fig. 3. When the junctions become significant, the equivalent circuits in Figs. 2 and 4 and their corresponding parameter

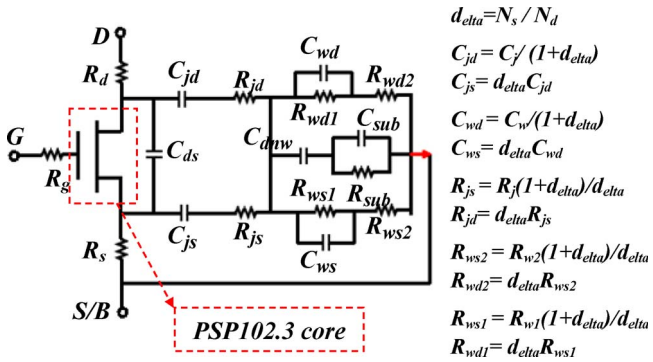

Fig. 4. Macromodel for DNW RF-MOSFET modeling when S/D junctions are not significant. All the parameters of the PSP102.3, including the terminal resistances R_d, R_g, and R_s, are beforehand extracted. The equations shown at the right side are used to calculate S-to-B and D-to-B components from the total extracted components, where N_s and N_d are the numbers of source and drain diffusion regions, respectively. When N_f is odd, $N_s = N_d = (N_f + 1)/2$, while $N_s = N_f/2 + 1$ and $N_d = N_f/2$ if N_f is even.

TABLE I
VALUES OF THE PARAMETERS EXTRACTED FROM SEVEN DEVICES WITH DIFFERENT N_f'S, AT $V_B = -1$ V AND $V_{\mathrm{SGD}} = 0$ V. ($L_f = 0.18\ \mu$m; $W_f = 5\ \mu$m)

Parameters \ N_f	1	2	4	8	16	32	64
C_j (*fF*)	7.42	11.4	18.4	33.1	62.3	118	238
R_j (10^3Ohm)	1.83	1.21	0.75	0.43	0.22	0.12	0.07
C_w (*fF*)	28.3	29.2	33.2	43.0	55.1	80.4	134
R_{w1} (Ohm)	520	351	266	216	144	97.6	53.4
R_{w2} (Ohm)	35.3	33.2	30.1	24.4	18.4	10.7	6.9
C_{dnw} (*fF*)	60.7	65.5	68.6	72.3	77.1	98.2	137
C_{sub} (*fF*)	14.6	14.2	14.4	15.2	15.7	16.8	18.9
R_{sub} (Ohm)	433	430	439	434	444	478	491
C_{sgcb} (*fF*)	28.2	34.3	32.5	46.4	59.8	90.2	151

values are less reasonable. Therefore, it is recommended that the C_j, R_j, C_w, R_{w1}, R_{w2}, C_{sub}, and R_{sub} be extracted at smaller than V_{jth}. The extraction of the substrate network parameters at $V_B < (V_{\mathrm{jth}} - 0.3\ \mathrm{V})$ and $V_{\mathrm{SGD}} = 0$ V gives a quite proper value. The parameter values extracted from the seven devices with different N_f's at $V_B = -1$ V and $V_{\mathrm{SGD}} = 0$ V are listed in Table I. To verify the validity of the proposed substrate network model and the extracted values, a macromodel (as shown in Fig. 4) for common-source-connected DNW RF MOSFET modeling was developed. The model that consists of PSP102.3 model core with the proposed new substrate network is simulated based on the extracted parameters in Agilent advanced design system directly. Fig. 5 shows an excellent agreement between the measured and simulated output admittances of the 16-finger DNW RF MOSFET at different operating regions, which verified that the model also holds for N_f ranging from 1 to 64. The C_{ds} in Fig. 4 is calculated from the de-embedded Y-parameters of the 16-finger nMOSFET as follows:

$$C_{ds} \approx \frac{\mathrm{Im}(Y_{22} - Y_{12})}{\omega} - \frac{C_{jd}(C_{js} + C_t)}{C_{jd} + C_{js} + C_t} \tag{10}$$

where $C_t = C_{wd} + C_{ws} + C_{\mathrm{dnw}}C_{\mathrm{sub}}/(C_{\mathrm{dnw}} + C_{\mathrm{sub}})$.

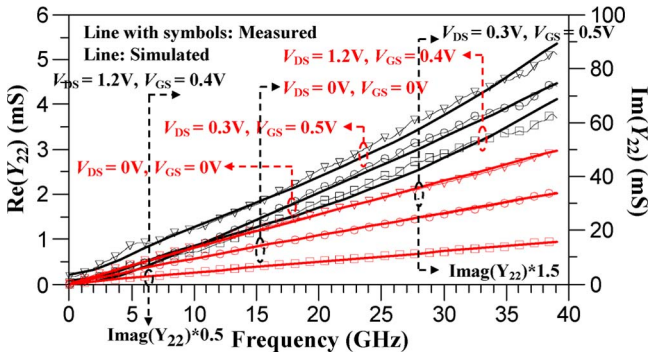

Fig. 5. Measured and simulated output admittances of the 16-finger DNW nMOSFET connected in a common-source configuration in different bias conditions.

IV. CONCLUSION

A simple test structure and a novel compact model have been presented for predicting the characteristics of the substrate network of DNW RF MOSFET. An analytical extraction algorithm has been presented for the substrate network parameters. The accuracy of the proposed method is validated through the excellent agreement observed up to 40 GHz between the simulated and measured output admittances of a 16-finger DNW RF MOSFET, connected in a common source and operated in different bias conditions.

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