IETE Technical Review

ISSN: 0256-4602 (Print) 0974-5971 (Online) Journal homepage: http://www.tandfonline.com/loi/titr20

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**To cite this article:** Chen Hu, Ming Li, Xiaoying He & Weifeng Sun (2011) A Review of Super Junction LDMOS, IETE Technical Review, 28:4, 327-335

**To link to this article:** http://dx.doi.org/10.4103/0256-4602.83553

Published online: 01 Sep 2014.

# A Review of Super Junction LDMOS

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## Abstract

Super Junction Lateral Double-diffused MOSFET (SJ-LDMOS) is one of the important attractive devices in high-voltage integrated circuit and power integrated circuit. However, the SJ-LDMOS is generally implemented on a low-resistance substrate, which always suffers from substrate-assisted depletion (SAD) effect, which thus degrades the performance of devices. A number of literatures have been published to solve the SAD effect and improve performance. This review summarizes the developments made in SJ-LDMOS based on bulk silicon, silicon on insulator, and silicon on sapphire in the last 10 years. Finally, the future work what researchers can do on the SJ-LDMOS also has been proposed.

**Keywords**

*Breakdown voltage, Bulk silicon, Lateral double-diffused MOSFET, Silicon on insulator, Silicon on sapphire, Specific on-resistance, Substrate assisted depletion, Super junction.*



## 1. Introduction

The RESURF technology has been greatly used in the Lateral Double-diffused metal–oxide–semiconductor field-effect transistor (MOSFET) (LDMOS) design since the concept was proposed in 1979 [1-2]. With RESURF technology, the excellent trade-off between the breakdown voltage (BV) and specific on-resistance can be obtained. Can we break through the conventional two-dimensional (2D) limitation of the relationship between on-resistance and BV? The answer is yes. This is the Super Junction (SJ) concept, which was proposed during the 1990s [3-5]. The SJ concept can be used to significantly reduce the resistance of the drift region in high-voltage Vertical Double-diffused MOS (VDMOS) or LDMOS for a given BV [6-11]. The typical cross-section of SJ-VDMOS and SJ-LDMOS can be seen in Figure 1. The SJ structure results in higher BV due to the charge compensation in the drift region (n pillars and p pillars), and lower on-resistance is achieved by highly doping the n pillars compared with the conventional DMOS. The SJ-VDMOS (CooLMOS) has recently become commercially available due to their technology improvements [7]. However, SJ-LDMOS devices have not materialized in spite of several years' investigation. This is partly due to the fact that the SJ-LDMOS suffers from the substrate-assisted depletion (SAD) effect, which reduces the BV. For SJ-LDMOS, shown in Figure 1(b), the p pillars are depleted by the two neighboring n pillars in the off-state, while n pillars are depleted by the two neighboring p pillars, as well as by the p substrate. This phenomenon is called the SAD effect. A vertical electric field component exists between the p substrate and n pillars, and the electric field is a function of the lateral position along the drift region and gives rise to a surplus of one type of charge in the pillars. The SAD effect is most significant near the drain.

The purpose of this article is to summarize the development of SJ-LDMOS based on bulk silicon, silicon on insulator (SOI), and silicon on sapphire (SOS) in the last 10 years. Subsequently, we discuss the future work that can be done on SJ-LDMOS.

## 2. Development of SJ-LDMOS

### 2.1 SJ-LDMOS on Bulk Silicon Substrate

In the SJ/RESURF LDMOS (SJR LDMOS) [12], the drift region is divided into an SJ region and a RESURF region, as illustrated in Figure 2. Because the SAD effect mostly occurs near the drain region, inserting the RESURF region with an appropriate doping concentration neutralizes this effect. The length and doping concentration of the RESURF region must be carefully chosen not only to suppress the depletion effects but also to maintain low on-resistance. A 605V, 87-m$\Omega\cdot$cm$^2$ SJ-LDMOS, with a structure similar to that of the above-mentioned SJR LDMOS, has also been reported earlier [13].

Figure 3 shows two different unbalanced SJ-LDMOS [14], which own a cell pitch of 10 μm and a length of 50 μm. Its SJ structure comprises five p type round pillars embedded, at an equal distance from one another, in the n type drift layer of 15-μm thickness down to the very thick, lightly doped p type substrate. Figure 3(a) is the uniform SJ-LDMOS, where all the round p pillars have the same diameter of 6 μm. Although such a uniform structure helps to equally distribute the surface electric field over the drift region, it is unable to efficiently suppress the SAD effect. For this purpose, the second non-uniform

SJ-LDMOS has been proposed, as shown in Figure 3(b). The round p pillars are arrayed with decreasing size from the channel to drain region. The diameter of the first p pillar near the channel is 7 μm, the last p pillar is 5 μm with diminishing in steps of 0.5 μm. This non-uniform configuration is supposed to counterbalance the gradient of space charge in the substrate during the blocking state. The simulation results reveal that the device with uniform SJ design has a fairly better trade-off between on-state resistance and BV. However, the BV of the non-uniform SJ device is much less influenced by charge imbalance in the SJ structure.

Figure 4 shows the Surface Low On-resistance Path (SLOP) SJ-LDMOS [15,16]. The key feature of this structure is that SJ primarily provides a low on-resistance path and is located at the surface of the drift region rather than the entire drift region, which is generally used in SJ devices to improve breakdown characteristics simultaneously. The manufacturing process of the device is relatively simple and compatible with the Bi-Complementary metal–oxide–semiconductor (CMOS) process. Three-dimensional (3D) device simulations indicate that the SLOP-LDMOS can provide a specific on-resistance reduction of 50% as compared with the conventional single RESURF LDMOS at a given BV. The proposed structure with a drift length of 15 μm is fabricated and demonstrated by using a modified CMOS process. The experimental result shows that the SLOP-LDMOS exhibits a BV of 250V and a specific on-resistance of 114 mΩ·cm$^2$.

Figure 5 shows the n-buffer SJ-LDMOS [17]. The key feature of the structure is the use of the n-buffer layer between the pillars and the underlying p substrate. As the drain voltage increases in the off-state, first the p pillars of the n-buffer SJ-LDMOST are depleted by the neighboring n pillars, as well as by the n buffer. The depletion between the p pillars and the n buffer causes reduction of the charge density in the p pillars, which compensates the lack of charge in the n pillars caused by the depletion between the n pillars and p substrate. The n pillars start to be affected by the p substrate after the n buffer is fully depleted at a high enough drain voltage. Once the n-buffer layer is fully depleted, the p pillars are no longer affected by the substrate. In the n-buffer structure, both pillars are affected by vertical depletion effects, while in the conventional SJ structure, only n pillars are affected. An n-buffer SJ-LDMOS, which is similar to the above n-buffer SJ-LDMOS, has also been reported [18]. The proposed structure with drift length of 3.5 μm is fabricated and demonstrated by using a 0.18 μm Bipolar-CMOS-DMOS (BCD) technology. The experimental result shows that the n-buffer SJ-LDMOS exhibits a BV of 98.6V and a specific on-resistance of 1.01 mΩ·cm$^2$, respectively.

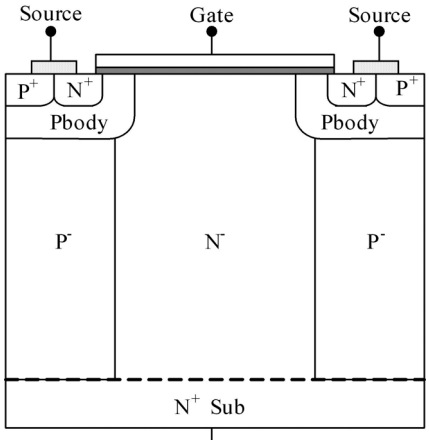


**Figure 1a:** Typical SJ-Device structures; Cross-section of SJ-VDMOS.

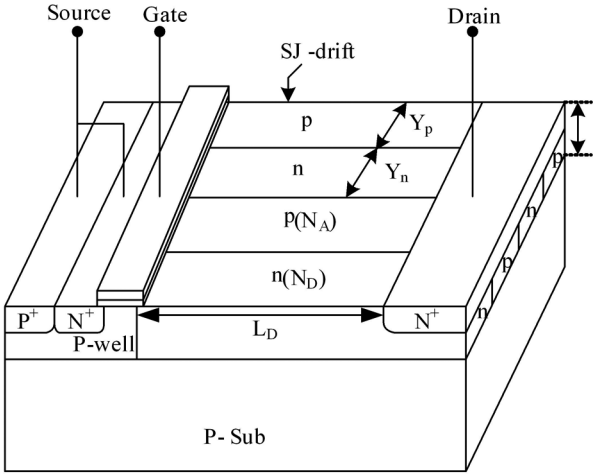


**Figure 1b:** Typical SJ-Device structures; 3D view of SJ-LDMOS.

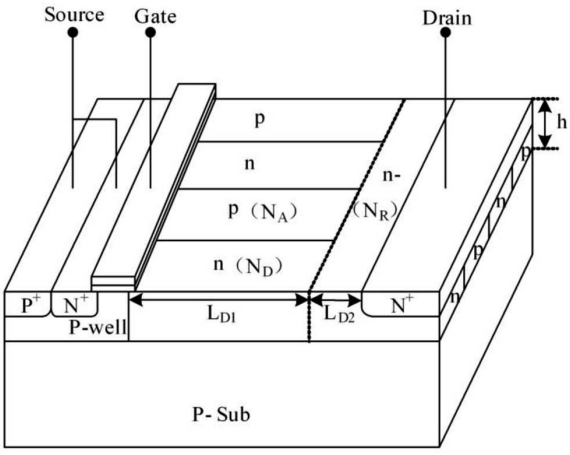


**Figure 2:** 3D view of SJR LDMOS.

Figure 6 shows the N$^+$-floating SJ-LDMOS [19]. The key feature of this structure is the use of the N$^+$-floating layer, whose concentration is more than $1 \times 10^{17}$ cm$^{-3}$. The distance from N$^+$-floating layer to the bottom of the drift

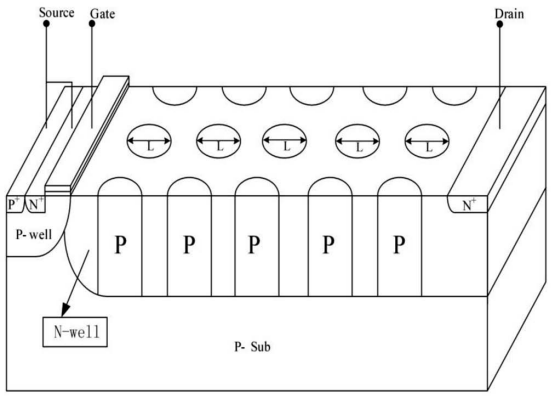


**Figure 3a:** 3D view of round uniform p-pillars SJ-LDMOS.

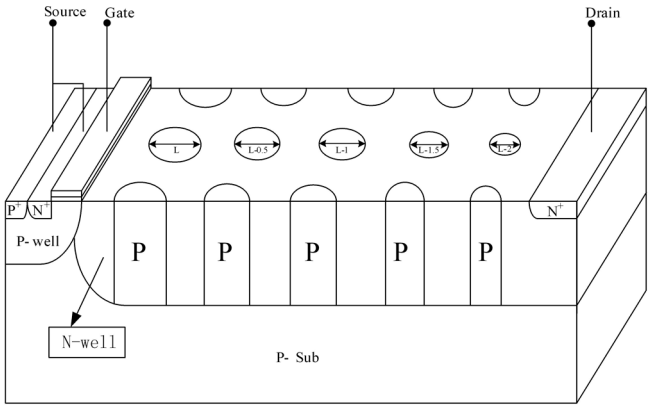


**Figure 3b:** Non-uniform p-pillars SJ-LDMOS.

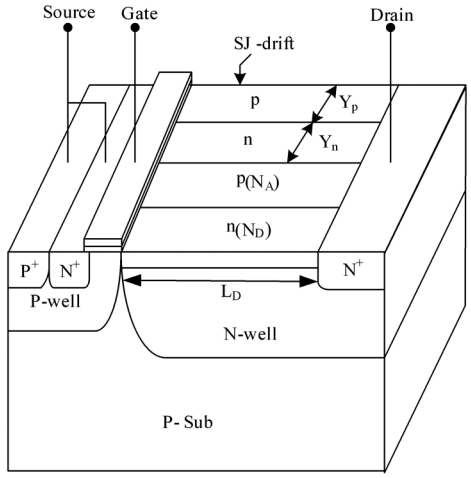


**Figure 4:** 3D view of SLOP LDMOS.

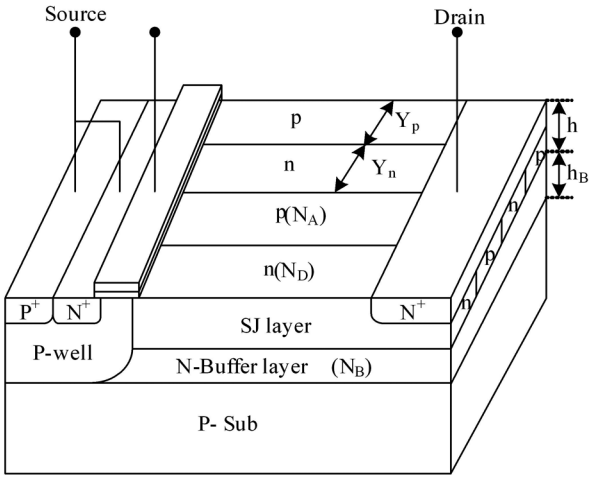


**Figure 5:** 3D view of n-buffer SJ-LDMOS.

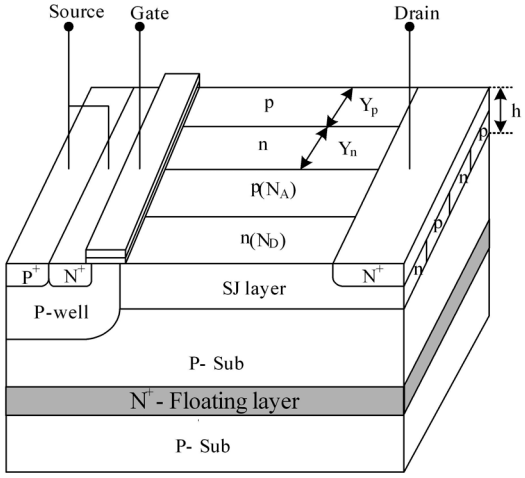


**Figure 6:** 3D view of N+-floating SJ-LDMOS.

region must be less than the thickness of the depletion layer in the substrate of the conventional SJ-LDMOS. As the drain voltage increases in the off-state, the n pillars of the $N^+$-floating SJ-LDMOST are depleted by neighboring p pillars, as well as by the p-type substrate above the $N^+$-floating layer. The p pillars start to be affected by the $N^+$-floating layer after the p substrate above the $N^+$-floating is fully depleted at a high enough drain voltage. In the $N^+$-floating SJ-LDMOST structure, both pillars are affected by vertical depletion effect, which causes a balance in charges between the pillars. The structure suppresses the SAD effect so as to achieve high BV, and, at the same time, maintains low on-resistance when the same length of drift region was applied.

An n-buried SJ-LDMOS structure with a partial n-buried layer between the p substrate and SJ pillars is illustrated in Figure 7 [20].The n-buried layer is implemented in order to suppress the SAD effect resulting in improving BV. This is due to the fact that the depletion between the p pillars and the n-buried layer causes a reduction in the charge density in the pillars, which is caused by the depletion between the n pillars and p substrate. The SAD effect is the most significant near the drain and less effective near the channel, as is evident from the equipotential contours for the conventional device. Therefore, the n-buried layer is only partial under the drain contact region, which is different from the n-buffer SJ-LDMOS,

where the n-buffer layer is under the entire drift region. Numerical simulation results in a BV of 188V in n-buried device compared with that of 85V and 145V in conventional SJ-LDMOS and n-buffer SJ-LDMOS, respectively.

Figure 8 shows the non-uniform n-buried SJ-LDMOS [21]. The key feature of the structure is that a non-uniform n-buried layer is implemented between the SJ region and p substrate, which provides a uniform distribution of surface electric field due to suppression of SAD and ensures the heavily doped n pillars extending over the entire drift region. The numerical simulation results indicate that the proposed device has high BV, low on-resistance, and can reduce sensitivity to doping imbalance in the pillars.

Figure 9 shows the new alternative n-buffer SJ-LDMOS [22]. The n-buffer is only located between the p pillars and the underlying p substrate and there are no n buffers under the n pillars. In this way, the concentration of the n pillars can be improved, so as to reduce the specific on-resistance.

Figure 10 shows the N-floating SJ-LDMOS [23], which has a partial n-type charge compensation layer implanted near the drain in p substrate. The obvious merit of this structure is a new electric field peak produced by the adding PN junction, which modulates the surface electric field distribution. Thus, the structure eliminates charge imbalance in order to achieve high BV while maintaining a lower on-resistance than that of the conventional SJ-LDMOS. The saturated BV of the N-floating SJ-LDMOS is higher than that of the n-buffer SJ-LDMOS, resulting from a more uniform surface electric field and reduced bulk field around the drain. Fabricated N-floating SJ-LDMOS with a drift region length of 35 μm and pillar width of 4.0 μm exhibits a specific on-resistance of 98 $m\Omega \cdot cm^2$ and BV of 410V, respectively.

Figure 11 shows a gradient SJ-LDMOS to overcome the SAD effect [24]. The height of the round p pillars are arrayed decreasingly from the channel to the drain region. The height of the first p pillar is equal to 10 μm, and the last p pillar is 8-μm high with the diminution in

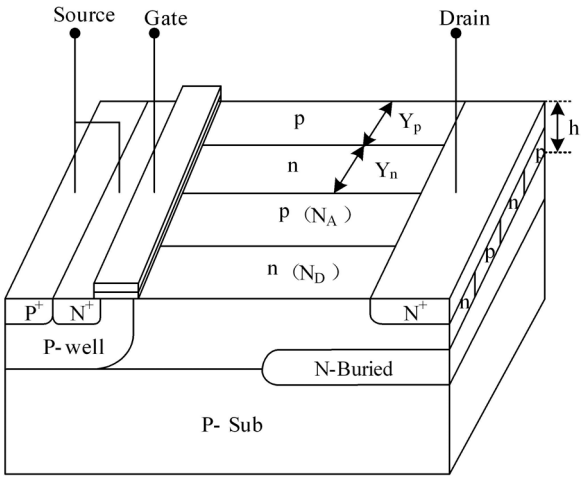


**Figure 7:** 3D view of n-buried SJ-LDMOS.

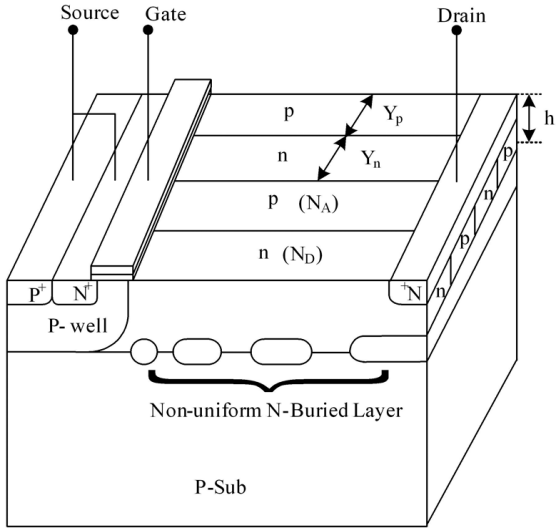


**Figure 8:** 3D view of non-uniform n-buried SJ-LDMOS.

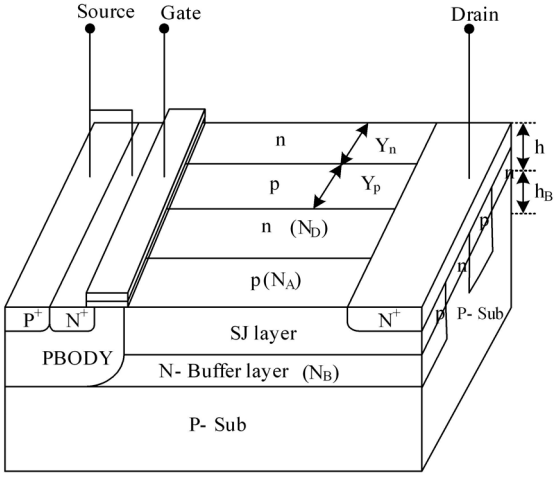


**Figure 9:** 3D view of alternate n-buffer SJ-LDMOS.

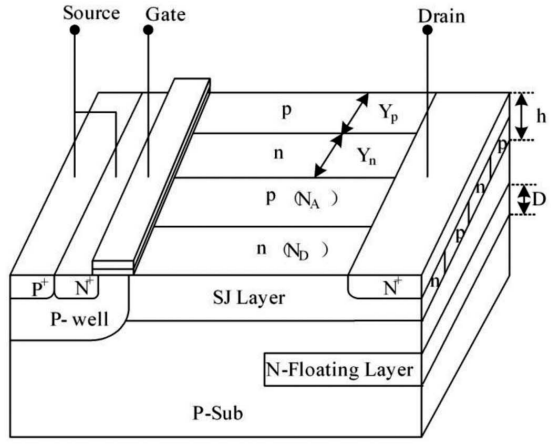


**Figure 10:** 3D view of N-Floating SJ-LDMOS

step of 0.5 µm. This structure increases the current path in the on-state and the concentration of n-drift region compared with the conventional structure. Therefore, the on-resistance is reduced.

### 2.2 SJ-LDMOS on SOI Substrate

SOI-LDMOS has better performance than LDMOS on bulk silicon [25-26], so the SJ-LDMOS on SOI material has been investigated in recent years. Figure 12 shows USJ-LDMOS on SOI [27]. The main feature here is the core diode structure outlined in bold. It consists of an alternately doped layer (n and p stripes) bounded at opposite ends by a $P^+$ and an $N^+$ region. The width of the n pillars increased toward the drain, and excess carriers in the n pillars compensate for the surplus of the space charge caused by the vertical interaction between the SOI, the buried oxide (BOX), and the underlying silicon substrate. In addition, a very thick BOX (>4 µm) can be regarded as a virtual insulating substrate so that the substrate effects are further reduced. As a result, the unbalanced SJ structure achieves nearly ideal simulated BV. A simulated device exhibits a BV of 700V and a specific on-resistance of 40 mΩ·cm$^2$.

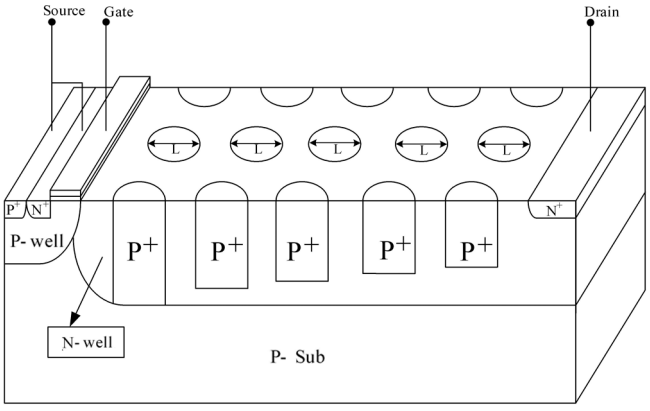


**Figure 11:** 3D view of gradient SJ-LDMOS.

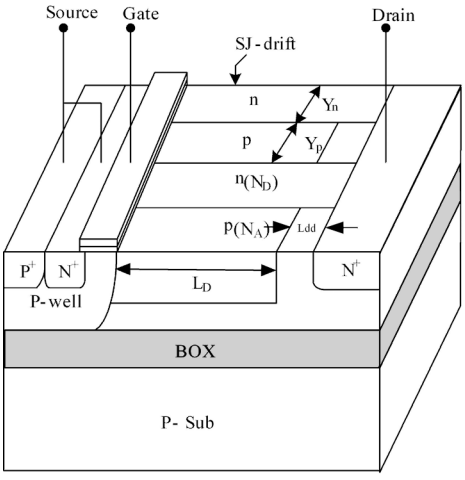


**Figure 13:** 3D view of SJR LDMOS on SOI.

The SJ/RESURF SOI-LDMOS is illustrated in Figure 13 [28]. The p layers (Ldd in Figure 13) are designed to leave a low n-doped region next to the $n^+$ drain, thus avoiding a high doping concentration gradient and a reduction in the electric field at the drain end of the drift region. The channel is obtained by lateral diffusion resulting in a graded profile with minimum doping concentration at the channel and the n-drift boundary, which reduces the concentration gradient in this region and further helps to reduce electric field crowding. The BV of the SJR LDMOS is 150V and the specific on-resistance is 1.65 mΩ·cm$^2$, respectively.

Using back-etched or membrane technology to remove the supporting silicon substrate can effectively eliminate the SAD effect in the devices, as shown in Figure 14 [29,30]. In this case, the SJ-LDMOS is implemented on an SOI wafer and the supporting substrate is removed by using anisotropic or reactive etching techniques. The BOX is used as an etch-stop. The removal of the substrate allows an ideal distribution of potential throughout the entire drift region. An experimental device with drift lengths of 15.5 µm [29] and 50 µm [30] exhibits the BV of 317 and 900V, respectively. However, the structures still exhibit relatively high on-resistance due to thin silicon film.

Figure 15 shows Partial SOI (PSOI)-LDMOS [31]. The SJ-LDMOS fabricated on the bulk silicon substrate suffers

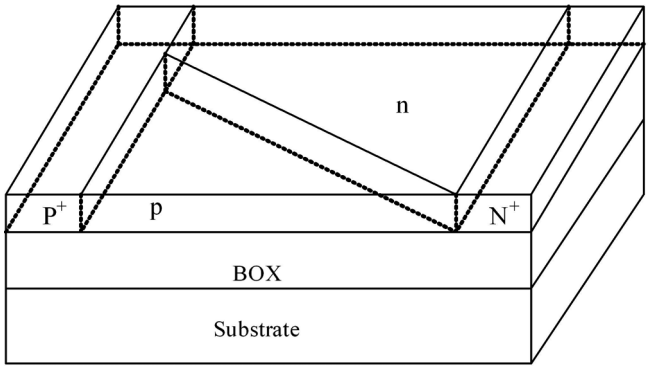


**Figure 12:** 3D view of USJ-LDMOS on SOI.

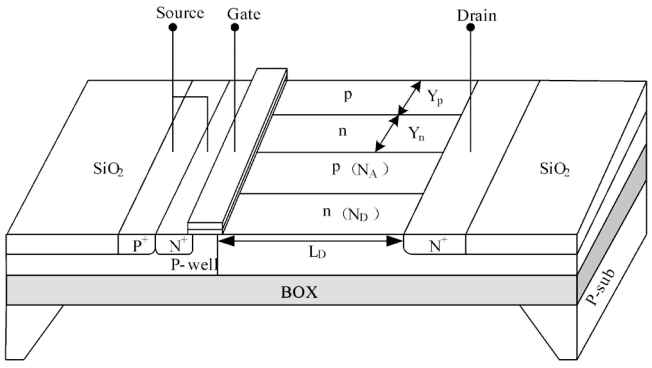


**Figure 14:** 3D view of BSJ LDMOS on SOI.

from the SAD effect, which causes charge imbalance, and thus limits the sustainable voltage rating. The device is fully integrated on the PSOI platform using the bulk silicon substrate. The new technology has the potential to eliminate the SAD effect. It enables implementation of SJ-LDMOS on bulk silicon substrate without sacrificing its electrical and thermal performance. The approach is demonstrated successfully on both planar and trench gate SJ-LDMOS devices. At the given BV rating, the drift region doping concentration can be raised to one order higher than that of the conventional LDMOS. The proposed technology has enabled fabrication of SJ power integrated circuits on the bulk silicon substrate for future automotive power electronics applications. The tested PSOI SJ-LDMOS exhibits a specific on-state resistance of 1.01 mΩ·cm$^2$, while the BV is 72.3V [31]. The trench gate PSOI SJ-LDMOS exhibits a BV of 96V and the specific on-state resistance of 2.64 mΩ·cm$^2$ [32].

Figure 16 shows the n-buffer SJ-LDMOS on PSOI [33]. The SJ structure consists of alternating n-type and p-type regions on the BOX layer, which are parallel to the direction of the applied electric field. The drift region constituted by the SJ structure is the same with conventional SOI SJ-LDMOS. The heavy doping ensures that voltage drop is very low and that the saturation current density is high at on-state. So the SJ structure constitutes the surface low on-resistance path. In the device, the buried oxide layer is removed partially at the drain region and n-buffer layer is implemented under the buried oxide layer. The n-buffer layer obtains drain voltage because of the opening of BOX in the drain region. The RESURF structure consisting of n-buffer/p-substrate sustains the blocking voltage at off-state. As a result, the SAD effect is reduced. The charge balance is achieved, which improves the electric field and increases the BV. In addition, the n-buffer layer increases the vertical BV without increasing the thickness of BOX. Numerical simulation results indicate that the BV of the proposed device with drift length of 15 μm is 280V.

The non-depletion compensation layer (NDCL) SJ-LDMOS on SOI [34], as shown in Figure 17, which consists of an alternation of N$^+$–oxide–P$^+$ structures, are implemented between the BOX and the SJ region. The dose of the P$^-$ buffer layer is very low, such that the NDCL is quickly depleted, achieving a linear potential distribution from the source to the drain region. The dose of both N$^+$ and P$^+$ in NDCL is high enough to keep their non-depletion at the device breakdown. The existing charges in the N$^+$ and P$^+$ of the NDCL can compensate for the n pillars, resulting in the charge balance between the n and p pillars of the SJ region while eliminating the SAD effects. In addition, the high-density oxide interface charges at the top surface of the BOX enhance the electric field in the BOX and improve the vertical BV. Numerical simulation results indicate that a uniform surface electric field profile is obtained and that the vertical electric field in BOX is increased to 6 × 10$^6$V/cm, which results in a high BV of 300V for the proposed device with the BOX thickness of 0.5 μm and drift length of 15 μm on a thin SOI substrate.

Figure 18 shows the SJ-LDMOS on SOI with added fixed charges on the BOX [35]. The SJ structure consists of alternating n- and p-type regions on BOX, which are parallel to the direction of the applied electric field. The drift region constituted by the SJ structure is the same as the conventional SOI SJ-LDMOS. The positive charges are implanted on the surface of BOX before the silicon direct bonding process. The added fixed charges are considered as the interface charge because the implanted ions are shallow and thin, which enhances the electric field and results in an increase in the vertical voltage in BOX. The added charges bear the vertical voltage with the BOX and induced electrons, which suppresses the SAD effect. By controlling the window size of the mask, the discrete charge distribution is approximately linear. The modulated vertical electric field suppresses the charge imbalance in SJ caused by the SAD effect, which

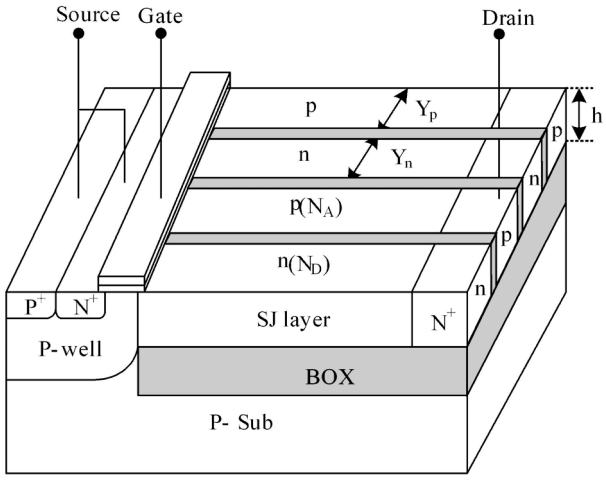


**Figure 15:** 3D view of PSOI SJ-LDMOS.

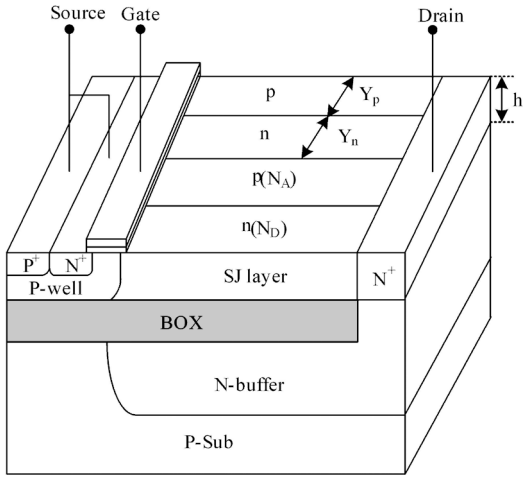


**Figure 16:** 3D view of n-buffer SJ-LDMOS on PSOI.

improves the BV. In addition, the enhanced electric field employs the thinner BOX, which is useful to minimize the self-heating effect. Simulation results indicate that the BV of the proposed device with the drift length of 10 µm is 223V.

### 2.3 SJ-LDMOS on SOS Substrate

Figure 19 shows SJ-LDMOS on silicon-on-sapphire (SOS) substrate [36-38]. The structure can eliminate the SAD effect. The device structure, including the SJ layer, is terminated by the insulating substrate (sapphire). The implementation of the SJ-LDMOS, apart from the creation of pillars, is carried out using an SOS CMOS compatible technology. The pillars are implemented using multiple high-energy ion implantations to reduce the thermal budget and minimize lateral diffusion of impurities. The uniformly doped vertical SJ pillars feature a width-to-height aspect ratio of 1.2 µm/0.7 µm. An experimental SJ-LDMOS with the drift region length of 66 µm and pillars' doping of $2\times10^{16}$ $cm^{-3}$ exhibits a BV of 520 V and a specific on-resistance of 0.82 Ω·$cm^2$ at $V_{GS}$ = 10V.

To further reduce pillar width in a 0.5 µm commercial CMOS/SOS technology, we propose the structure illustrated in Figure 20 [37]. In this structure, compensated regions exist due to overlapping of n and p pillars, resulting in a pillar height-to-width ratio of 0.12 µm/0.3 µm. An experimental device, with a drift region length of 10 µm and pillar doping of $2\times10^{17}$ $cm^{-3}$, exhibits a BV of 170V, with an average lateral electric field at breakdown of 17V/µm, which is roughly equal to the critical electric field. Although nearly ideal BV is obtained using SOS substrates, the specific on-resistance is relatively higher than that of the conventional RESURF LDMOS due to the very thin silicon layer inherent in SOS technology.

## 3. Conclusion and Future Work

In this paper, various SJ-LDMOS structures on bulk silicon, SOI, and SOS materials have been explored. The SAD effect, which is one of the most important issues, has also been discussed in detail. Briefly, the idea of reducing or eliminating the SAD effect is by decreasing the influence of substrate on the drift region. For SJ-

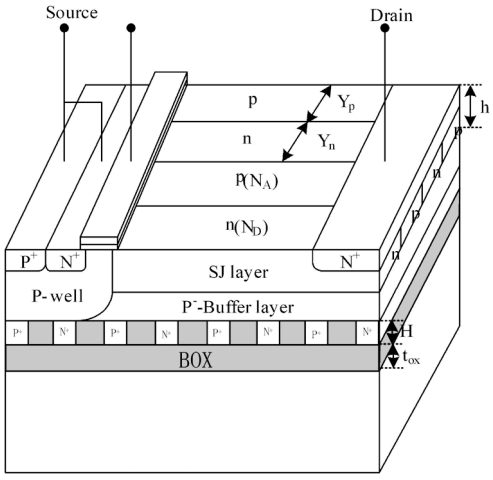


**Figure 17:** 3D view of NDCL SJ-LDMOS on SOI.

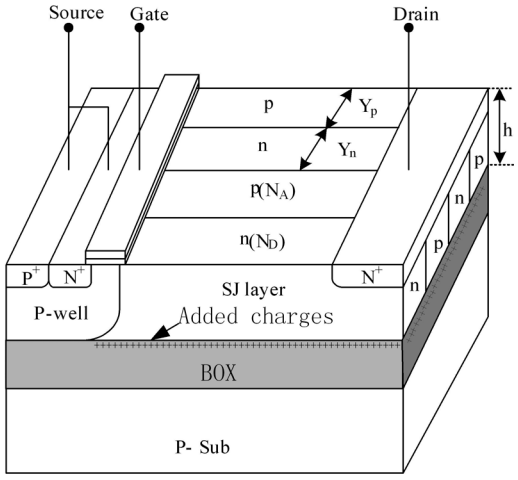


**Figure 18:** 3D view of charged BOX SJ-LDMOS on SOI.

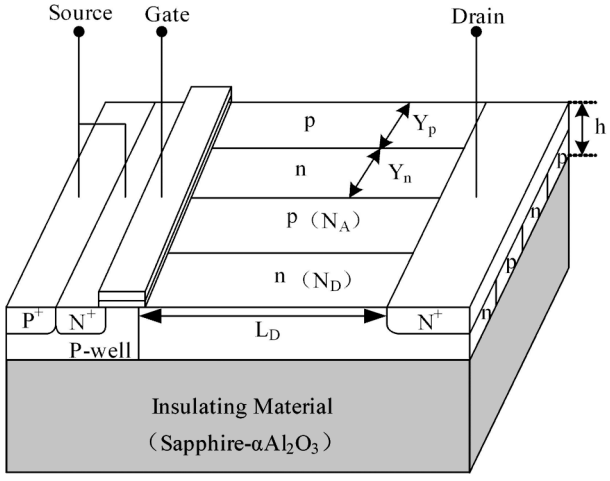


**Figure 19:** 3D view of SJ-LDMOS on SOS.

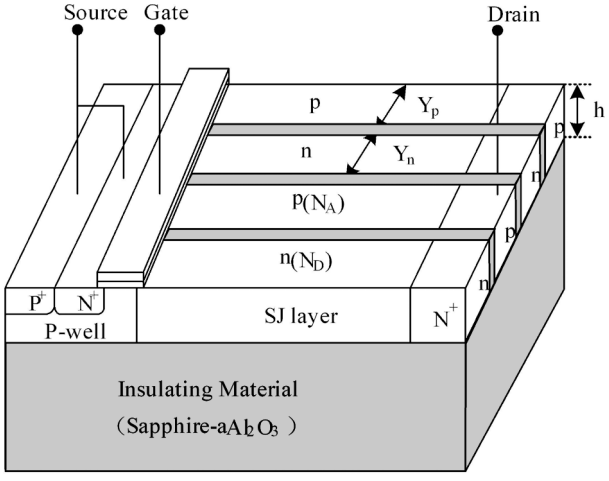


**Figure 20:** 3D view of overlapping SJ-LDMOS on SOS.

**Table.1 The experimental performance of the SJ-LDMOS**

| Device | Breakdown voltage (V) | $R_{ON,SP}$ ($m\Omega \cdot cm^2$) | FOM=$BV^2/R_{ON,SP}$ |
|---|---|---|---|
| SJR SJ-LDMOS on bulk silicon [13] | 605 | 87 | $4.21\times10^6$ |
| SLOP SJ-LDMOS on bulk silicon [15] | 250 | 114 | $5.48\times10^5$ |
| n-buffer SJ-LDMOS on bulk silicon [18] | 98.6 | 1.01 | $9.63\times10^6$ |
| PSOI SJ-LDMOS [29] | 72.3 | 1.01 | $5.18\times10^6$ |
| SJR SJ-LDMOS on SOI [26] | 150 | 1.65 | $1.36\times10^7$ |

LDMOS on the bulk-silicon substrate, there are vertical PN junctions between the n-drift and p substrate. The potential of the drift region gradually decreases from drain to source. Hence, we can increase the concentration of n-drift region near the drain to compensate the depletion by the p substrate, such as N-buried SJ-LDMOS. Another way is to increase a PN junction near the drain in p substrate to reduce the influence of p substrate on the n-drift, such as N-floating SJ-LDMOS. For SJ-LDMOS on the SOI substrate, we can increase the thickness of BOX layer to reduce the influence of SAD effect, such as PSOI SJ-LDMOS, which also has resolved the thermal dissipation issue. Another method is to add the PN junction above the BOX layer to achieve a linear potential distribution from the source to drain region, such as NDCL SJ-LDMOS. For SJ-LDMOS on the SOS substrate, the substrate is an insulator, so the SAD effect can be fully eliminated.

Table 1 shows the experimental performances of the SJ-LDMOS. As illustrated, the n-buffer SJ-LDMOS has the best FOM ($BV^2/R_{ON,SP}$) on bulk silicon material. The SAD effect can be better suppressed on SOI substrate, so that the SJ-LDMOS on SOI has better FOM than that on bulk silicon. Although other SJ structures have better FOM from the simulation results, no experiment results are concluded. Except that various novel SJ-LDMOS should be experimented on, the following work also should be carried out:

(1) For SJ-LDMOS on bulk-silicon and SOI material, there has been a large number of researches on overcoming the SAD effect. The experimental results also have shown that the characteristics of SJ-LDMOS are better than the conventional RESURF LDMOS. The work that should be done next is technology integration, ie, the SJ-LDMOS should be integrated into the standard CMOS or BiCMOS process for power integrated circuits (ICs). Large numbers of trade-off should be done between the performance and cost before the SJ-LDMOS can be really applied in power IC products.
(2) The next study that we can do is reliability issues on SJ-LDMOS. Because the current density of SJ-LDMOS is larger than the conventional LDMOS, the self-heating effect and hot carrier effect may be serious and the Safe-Operation-Area (SOA) may be smaller. Certainly, there are many other reliability issues, such as Time-Dependent Dielectric Breakdown (TDDB) and Negative Bias Temperature Instability (NBTI), etc. The reliability issues also should be resolved before SJ-LDMOS indeed becomes a product and is industrialized.
(3) There are less number of literature available on how to realize the SJ-LDMOS on wide bandgap semiconductor materials (eg, SiC, GaN, etc). Also, the SAD effect and reliability issues have not been investigated as yet.

## 4. ACKNOWLEDGMENTS

The authors would like to thank the New Century Excellent Talents in University Program (NCET-10-0331) for the project.

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DOI: 10.4103/0256-4602.83553; Paper No. TR 112_11; Copyright © 2011 by the IETE