DESIGN OF ASYMMETRICAL SPURLINE FILTER FOR A HIGH POWER SiC MESFET CLASS-E POWER AMPLIFIER

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ABSTRACT: *An asymmetrical spurline filter (ASF) with dual-bandgap characteristics is designed and applied as the load network of the class-E power amplifier to improve the output power and efficiency. Meanwhile, an equivalent circuit model is built for the proposed ASF based on two LCR resonators.* © 2010 Wiley Periodicals, Inc. Microwave Opt Technol Lett 52: 1650–1652, 2010; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.25260

Key words: *asymmetrical spurline filter; class-E power amplifier; harmonics suppression; high output power; SiC MESFET*

1. INTRODUCTION

As promising candidates for reducing the consumption of communication equipment, class-E power amplifiers (PAs), first introduced in 1975 [1], have been widespread applied in current communication systems due to their design simplicity and high efficiency. Meanwhile, in many wireless communication applications, such as mobile phones, it is critical to minimize harmonics distortion and size of PAs with requirements of high output power and efficiency [2]. Understandably, load networks with harmonics suppression and compact size are attractive to class-E PA designers. The transmission-line load network topology proposed in [3], which consists of six transmission-lines to suppress five-order harmonics, has been successfully adopted in class-E PA designs [4–5].

Spurline filters, first introduced in [6], are potential solutions to harmonic suppression in PAs due to their inherent merits including simple structure, small size, and low cost. As passive component, spurline filters can be simply realized by etching L-shape slots on microstrip lines, and provide bandgap characteristics without any other stubs and etched processing on backside ground plane [7, 8].

In this letter, we propose a high power class-E PA with an asymmetrical spurline filter (ASF) as the load network to suppress harmonics for the first time. The silicon carbide (SiC) metal-semiconductor field effects transistors (MESFET) is adopted as an active device to achieve better performance. The results suggest that the proposed ASF is effective in suppressing the harmonics of the class-E PA.

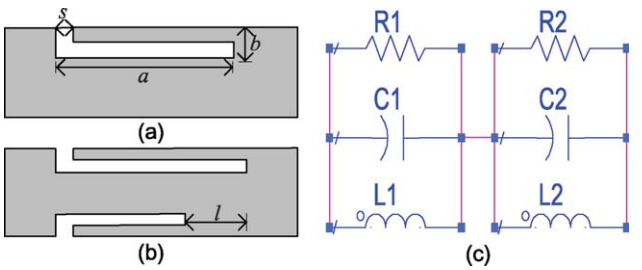

Figure 1 (a) The conventional single spurline filter. (b) The asymmetrical spurline filter. (c) The circuit model of the asymmetrical spurline filter. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

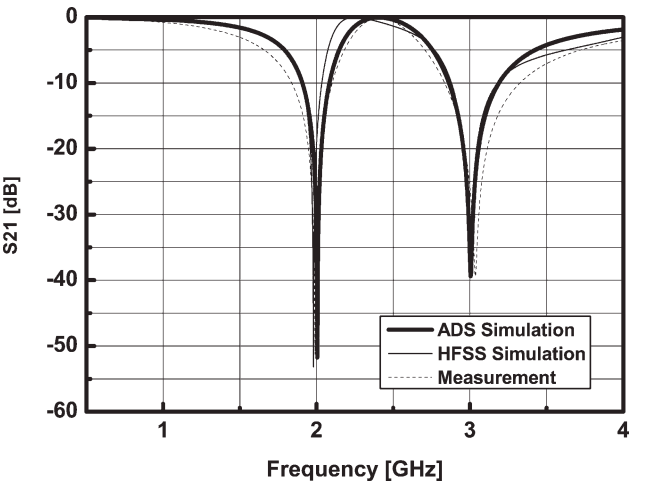

Figure 2 The insertion loss of proposed asymmetrical spurline filter

2. THE ASF DESIGN

The configuration of a conventional single spurline filter is shown in Figure 1(a), which is composed of a microstrip line and an L-shape slot. As the slotted line demonstrates an inductive effect and the slot gap performs a capacitive effect, the spurline filters can provide band-gap characteristics. Its cut-off frequency is determined by three parameters: slot width s, slot length a, and slot height b. The required cut-off frequency can be obtained by adjusting the above three parameters. When another slot with different slot length is embedded into the single spurline filter as shown in Figure 1(b), the filter called ASF can provide two distinct cut-off frequencies. The distance between the two frequencies is mainly decided by the l, which is the difference of the two slot lengths. By adjusting the values of s, a, b, and l, arbitrary two cut-off frequencies can be obtained [7].

Furthermore, a circuit model for the ASF is presented in Figure 1(c). The resonator circuits L_1C_1 and L_2C_2 represent the dual-bandgap characteristics, and the resistors $R_1$and R_2 are included to represent the radiation effect and transmission loss. The circuit parameters can be obtained from following equations [7, 9].

$$R_i = 2Z_0(1/|S_{21,i}| - 1)|_{f=f_i} \quad (1)$$

$$C_i = \sqrt{0.5(R_i + 2Z_0)^2 - 4Z_0^2}/2.83\pi 2Z_0R_i\Delta f_i \quad (2)$$

$$L_i = 1/4(\pi f_0)^2C_i \quad i = 1, 2 \quad (3)$$

where Z_0 is the characteristic impedance of the transmission line, f_i is the resonant frequency, $S_{21,i}$ is the insertion loss, and Δf_i is the -3 dB bandwidth of S_{21} at f_i.

For verification, an ASF was designed, fabricated, and measured. The proposed ASF was etched on a 50 Ω transmission

TABLE 1 Values of Circuit Parameters

$R1$	$C1$	$L1$	$R2$	$C2$	$L2$
79.42 kΩ	1.2pF	5.3 nH	18.46 kΩ	0.55 pF	5.12 nH

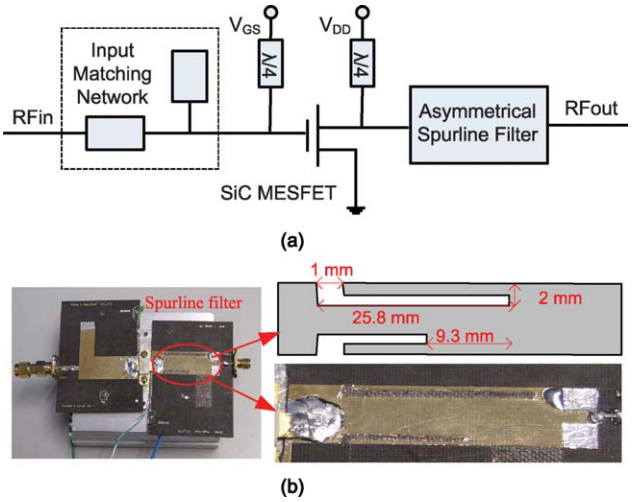

Figure 3 (a) The full schematic of the proposed class-E PA. (b) Photograph of the proposed class-E PA. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

line, and the substrate has a relative dielectric constant 2.65 with a thickness of 1 mm. According to the layout shown in Figure 1(b), the dimensions of the ASF are as follows: $s = 1$ mm, $a = 25.8$ mm, $b = 2$ mm, and $l = 9.3$ mm. Simulations were first carried on the Ansoft HFSS 11.0 to acquire the insertion loss characteristics of the ASF. As shown in Figure 2, the ASF provides two cut-off frequencies at 2 and 3 GHz.

Based on the HFSS simulation results in Figure 2 with (1), (2), and (3), the circuit parameters $R1$, $C1$, $L1$, $R2$, $C2$, and $L2$ are 79.42 kΩ, 1.2 pF, 5.3 nH, 18.46 kΩ, 0.55 pF, and 5.12 nH' listing in Table 1. The circuit model is simulated in the Agilent advanced design system (ADS), and the results are also showed in Figure 2. From 0.5 to 4 GHz, the ADS simulation results present a good agreement with the HFSS simulation results. This demonstrates the validity of the circuit model. Figure 2 also includes the measurement results of the ASF tested by the network analyzer Agilent E5071B.

3. THE CLASS-E POWER AMPLIFIER DESIGN

The basic principle of the class-E PA has been described in [1, 2]. The theoretical drain efficiency of 100% can be achieved by avoiding the high drain voltage and the high drain current across the device simultaneously. Figure 3(a) shows the full schematic of the proposed class-E PA using an ASF as load network, which was implemented with Cree CRF24060 60-W SiC MESFET. Figure 3(b) shows the photograph of the proposed PA. It can be seen that the structure is considerably more simple and compact, which is convenient for simulating and measuring. In the class-E PA, the transistor operates as an on-to-off switch and the drain voltage waveform is determined by the switch when it is turned on and by the transient response of the load network when the switch is turned off. Therefore, the load network is not just for matching the 50 Ω load resistance but also for adjusting the phase of drain voltage and current to make them orthogonal to achieve high output power and PAE. By using load-pull tool in ADS, the optimum output impedance 7.5 + j3.7 was easily obtained.

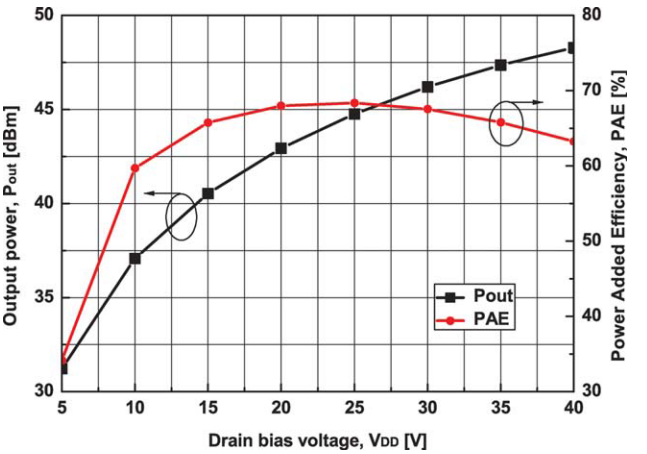

Figure 5 Output power and PAE characteristics according to drain bias voltage. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

4. SIMULATED AND MEASURED RESULTS

Simulations were run to optimize the performance of the proposed class-E PA. Figures 4 and 5 show the simulated characteristics of output power level and PAE of the class-E PA as a function of gate and drain bias voltages for an input power (P_{in}) of 35 dBm, respectively. Figure 4 suggests that the maximum

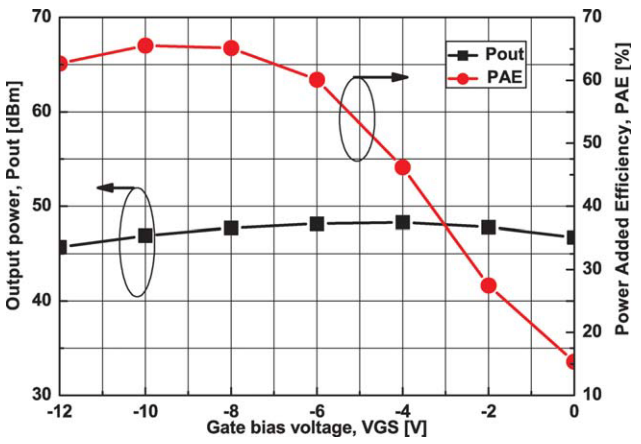

Figure 4 Output power and PAE characteristics according to gate bias voltage. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

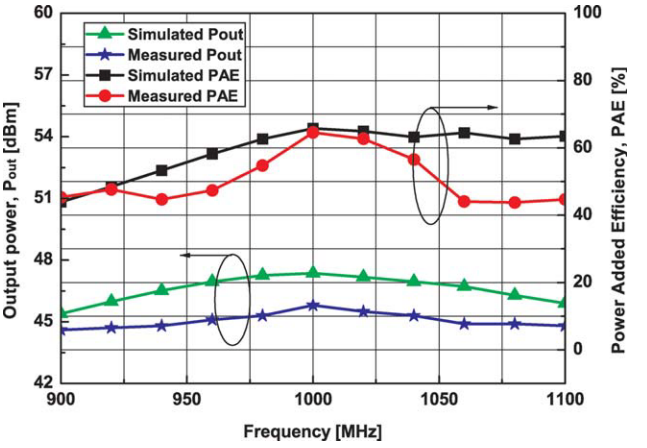

Figure 6 Output power and PAE characteristics according to frequency. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

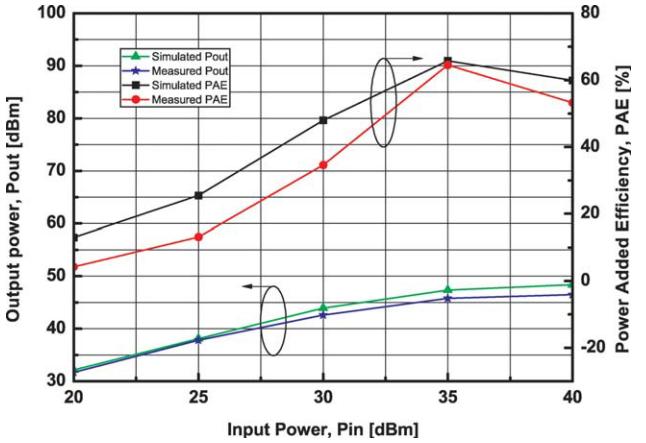

Figure 7 Output power and PAE characteristics according to input power. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

output power can be achieved when the gate bias voltage (VGS) is −4 V. However, the PAE decreases dramatically when VGS above −9 V. As a result, VGS = −9V is the optimal choice in consideration of the trade-off between efficiency and output power. In Figure 5, it can be seen that the high PAE characteristics are maintained for a drain voltage variation of 20 V that is from 15 V to 35 V. On the other hand, the output power increases linearly according to the drain bias voltage (VDD). Thus, to achieve relative high PAE and high output power, VGS = −9 V and VDD = 35 V were selected in simulation and measurement.

The output power and PAE characteristics versus frequencies curves are shown in Figure 6 for a P_{in} of 35 dBm. Figure 7 shows the simulated and measured output power and PAE characteristics according to change of the input power at 1 GHz. The simulation and experimental results are similar except a little decline. Both figures indicate that a highest output power and PAE were achieved at 1 GHz for a P_{in} of 35 dBm. The maximum measured output power and PAE are 45.8 dBm and 64.6%.

There is a saturation value of PAE to confirm switch mode of operating, because the on-state resistance of the active device will limit the maximum achievable drain efficiency. Specifically, the maximum achievable drain efficiency depends on ratios between the on-state resistance, output capacity of transistor, supply voltage, and output power. Increasing the output power for a given drain voltage proportionally increases the drain current, and the voltage drop across the device on-state resistance also increases, resulting in decrease of the drain efficiency of the proposed PA. Therefore, it is can be explained that the proposed PA owns a high output power but low PAE [4, 10].

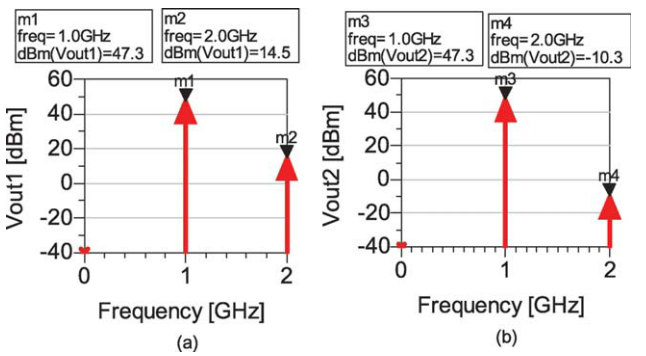

Figure 8 Simulated results of the output voltage of the class-E PA with (a) a normal load network. (b) an symmetrical spurline filter as the load network. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

TABLE 2 Performance Comparison

Work	Frequency	Max. spout (dBm)	Max. PAE (%)
[4]	Broadband	34	45
[5]	2.14 GHz	40	72.30
[10]	145 MHz	43.1	83.50
This work	1 GHz	45.8	64.60

Figure 8 is the simulated results of V_{out1}, which is the output voltage of a class-E PA using a load network topology proposed in [3] and V_{out2}, which is the output voltage of a class-E PA with an ASF as load network. Compared with V_{out1}, the second harmonic of V_{out2} is 24.8 dBm less, which demonstrates that the ASF can suppress the harmonics effectively.

Table 2 shows performance comparison with other reference works. By using an ASF as the load network, the proposed class-E PA shows comparable performance.

5. CONCLUSIONS

In this letter, a high output power class-E PA using a SiC MESFET was designed and implemented at 1 GHz. An ASF is applied as the load network for the first time to improve the performance of the proposed PA. The proposed ASF has dual-bandgap characteristics, which owns 2 and 3 GHz two cut-off frequencies. The measurement results were in a good agreement with simulation results except some insignificant distinctions. At 35 V drain bias and −9 V VGSs, the output power of 45.8 dBm was achieved with the maximum PAE of 64.6% at a P_{in} of 35 dBm. The experimental results suggest that the compact ASF is effective to harmonic suppression for microstrip circuit applications.

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