A Single-Chip CMOS UHF RFID Reader Transceiver for Chinese Mobile Applications

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***Abstract*—UHF RFID reader transceiver for Chinese local standard (840–845 MHz and 920–925 MHz), in concord with the protocols of EPC Class-1 Gen-2 and ISO/IEC 18000–6C, is presented. A highly linear RF front-end with low flicker noise, an on-chip self-jammer cancellation (SC) circuit with fast time-varying cut-off frequency and a DC-offset cancellation (DCOC) circuit are proposed to deal with the large self-jammer in the receiver. In the presence of 22 dBm PA output power, the receiver achieves a sensitivity of −79 dBm including the 15 dB loss of the directional coupler. A CMOS class-AB PA is integrated in the transmitter, with 22 dBm output power and 35% PAE. The spectrum mask achieves $ACPR_1$ of −45 dBc and $ACPR_2$ of −60 dBc. A sigma-delta fractional-N PLL with a single *LC* VCO is also implemented for good phase noise (−126 dBc/Hz @ 1 MHz offset) and high frequency resolution within 1 kHz. This single-chip is fabricated in a 0.18 μm standard CMOS process. It occupies a silicon area of 13.5 mm^2 and dissipates 203 mW from a 1.8 V supply voltage when transmitting 7.5 dBm output power.**

***Index Terms*—Chinese RFID reader, CMOS transceiver, DCOC, mobile RFID reader, reader, RFID, self-jammer, transceiver, transmitter leakage, UHF RFID reader.**

I. Introduction

RADIO-FREQUENCY identification (RFID) is growing rapidly and expected to be the most promising choice for automatic identification applications. The ubiquitous barcode has dominated the identification system for many years. However, once the cost of the RFID tags, especially the passive tags, approaches the cost of the barcode labels, RFID may replace the barcode and arouse other potential applications, such as supply chain management, purchasing, distribution industries and so on [1]. Obviously, the RFID tags have several advantages, including contactless, long read range, high data rate, large information storage, ability of rewritable, and so on.

Compared to the near-field inductive coupled RFID systems operating at the low frequency (LF) of 125 kHz or 134 kHz and the high frequency (HF) of 13.56 MHz, the ultra high frequency (UHF) RFID systems are gaining worldwide momentum. These reader systems are operating at the Industrial-Scientific–Medical (ISM) band around 900 MHz, and have advantages of longer read distance up to 10 m, larger information storage, and faster data rate up to 640 kbps [2], [3]. Because of the higher operation frequency, the UHF RFID readers and tags have smaller size of antennas beneficial for high integration. On the other hand, the UHF RFID readers with high integration, low cost, and low power, are suitable for the mobile handsets. Thus, they are very promising for integrated into the mobile cellular and wireless network terminals to arouse lots of new applications. For instance, we are able to use the mobile phones to access the information of the products conveniently. The terminals integrated with the readers and GPS receivers or other wireless modules can supervise, locate and track the products seamlessly, which would greatly enhance the efficiency of the supply chain management.

The existing UHF RFID readers based on discrete components have been fully developed, but they are bulky, expensive, and large power consuming. A single-chip reader implemented in 0.18 μm SiGe BiCMOS reported in [4] achieves good sensitivity in the presence of large self-jammer. However, it utilizes off-chip capacitors to handle the DC leakage, and consumes large power of 1.5 W. A highly linear, low power CMOS reader with on-chip scheme of canceling the self-jammer is reported in [5], but the sensitivity is limited to the bad noise performance. Furthermore, most of the existing single-chip UHF RFID reader transceivers [4]–[7] are not able to meet the Chinese local standard, whereas the huge Chinese market has a urgent demand for RFID reader systems, especially the mobile readers.

This paper describes a single-chip CMOS UHF RFID reader transceiver for Chinese mobile applications, which achieves low power consumption (203 mW) and high integration. In the presence of 22 dBm transmitter power, it realizes a sensitivity of −79 dBm including the 15 dB loss of the directional coupler. A highly linear active RF front-end in the receiver successfully tolerates the large self-jammer, and an on-chip self-jammer cancellation (SC) circuit and DC offset correction (DCOC) circuit are proposed to remove the large DC leakage. Additionally, an integrated CMOS class-AB PA has a maximum output power

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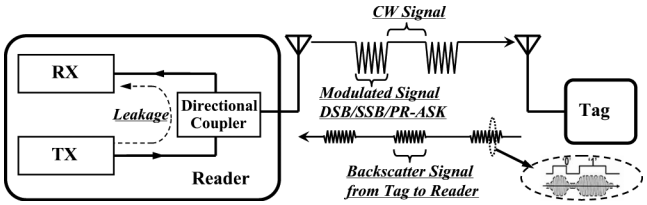


Fig. 1. UHF RFID system.

of 22 dBm and power-added efficiency (PAE) of 35%, which is suitable for the mobile applications. The chip can also drive an external PA to deliver an output power up to 30 dBm for the longer communication distance. This reader supports the protocols of EPC class-1 generation-2 [2] and ISO/IEC 18000–6C [3], as well as the Chinese standard [8]. It also meets the spectrum regulation of Chinese local requirements [8], which are more stringent than the ETSI EN 302 208–1 [9] in Europe and the FCC Title 47, Part 15 [10] in the USA.

The paper is organized as follows. Section II describes the system design considerations and the main challenges in the UHF RFID reader design, together with the existing solutions and their limitations. Section III presents the system architecture and specifications. The details of the circuit implementation are discussed in Section IV. Section V shows the measurement results and a conclusion is presented in Section VI.

II. System Considerations and Challenges

In passive UHF RFID system, the tags need to get the power from the reader. As illustrated in Fig. 1, the reader first transmits the continuous-wave (CW) signal to activate and "power up" the tag, and then the tag returns the wanted signal to the reader by backscattering the CW signal. If the tag is the corresponding one, the communication link between the reader and the tag will be established. Then the reader sends the DSB/SSB/PR-ASK modulated signal to command the tag, and subsequently transmits the CW signal to keep the tag energized. At the same time, the reader listens to the backscattered signal from the tags. It is to be emphasized that the transmitter is keeping transmitting the CW signal, during the receiving of the wanted signal. Therefore, with the transmitter and the receiver sharing a single antenna, the receiver must tolerate the large leakage signal (self-jammer) from the transmitter, because of the limited isolation. Typically, this self-jammer is much larger (over 10 dBm) than the wanted signal (down to -80 dBm), and unfortunately falls in the middle of the wanted signal band. It leads to several problems as follows.

A. Blocking by the Self-Jammer

The large self-jammer would saturate the RF front-end in the receiver and block the wanted signal. To decrease the self-jammer, a directional coupler is utilized in our design to decrease the self-jammer for relaxing the linearity requirements of the RF front-end. Although it has 15 dB loss in sensitivity, it is still acceptable and worthwhile for the system. Even so, the self-jammer is about -5 dBm when transmitter delivers a 30 dBm power, which is still much larger than the wanted signal. On the other hand, the removal of the self-jammer is required to be fast enough to meet the requirements of the transmit-to-receive turn-around time [2]. Thus, to rapidly remove the self-jammer without the wanted signal is a crucial challenge in the reader design.

A method to kill the self-jammer in RF domain is proposed in [11], which utilizes two RF paths to subtract the self-jammer by an auxiliary path. Nevertheless, since it highly depends on the perfect phase and gain matching between the two paths, it might not be feasible. Thus, most reader designers adopt the direct-conversion architecture to down-convert the self-jammer to DC leakage for removal. But it needs to live with the self-jammer in RF domain, which highly requires the sufficient linearity for RF front-end. A highly linear passive mixer without low-noise amplifier (LNA) in CMOS technology is realized in [5], but the sensitivity is not good due to the poor noise performance. Instead, another active mixer is implemented in [4] to achieve the sufficient linearity and good sensitivity, but it is based on the SiGe BiCMOS and a 5 V supply voltage is needed. In this work, we implemented an active highly linear RF front-end to make a good tradeoff between linearity and sensitivity to achieve optimal performance.

Under the DC frequency, several schemes [4]–[7] were proposed to remove the DC leakage. A self-jammer cancellation circuit with off-chip capacitors is employed in [4] to remove the DC leakage. However, the fully differential I/Q receiver needs four off-chip capacitors and eight pins in the package. Another scheme reported in [5] is based on the on-chip DCOC circuit to remove the leakage, but the settling time might become longer when the DC leakage is larger. Regarding these aspects, we proposed an on-chip SC circuit with quickly time-varying cut-off frequency and on-chip DCOC circuit to kill the DC leakage.

B. Phase Noise of the CW Signal

The phase noise of the CW signal will also leak into the receiver together with the self-jammer. It would flood the wanted signal since the self-jammer is much larger than the wanted signal. Thus, reference [12] regarded it as a serious problem and deal with it through the leakage canceller in the RF domain.

However, the challenge of the phase noise of the CW signal can be well handled by adopting the same LO in the transmitter and receiver. The correlated phase noise of the CW signal and LO can be self-mixed down to DC leakage, which can be removed by the SC and DCOC circuit. The level of DC leakage is determined by the phase difference between the two paths. As the CW signal becomes larger, the nonlinearity of the transmitter would introduce more phase noise mismatch, corresponding to more noise in the receiver. Hence, in order to avoid degrading the sensitivity, the receiver could adopt the CW signal from the transmitter as the LO signal to maintain the high correlation of the phase noise.

C. Transmitter Noise

Similar to the phase noise of the CW signal, the transmitter noise associated with the self-jammer will also leak into the receiver. When the self-jammer is large enough, the transmitter noise would exceed the noise floor and deteriorate the sensitivity of the receiver. Thus, a sufficient signal-to-noise ratio (SNR) of the CW signal should be guaranteed.

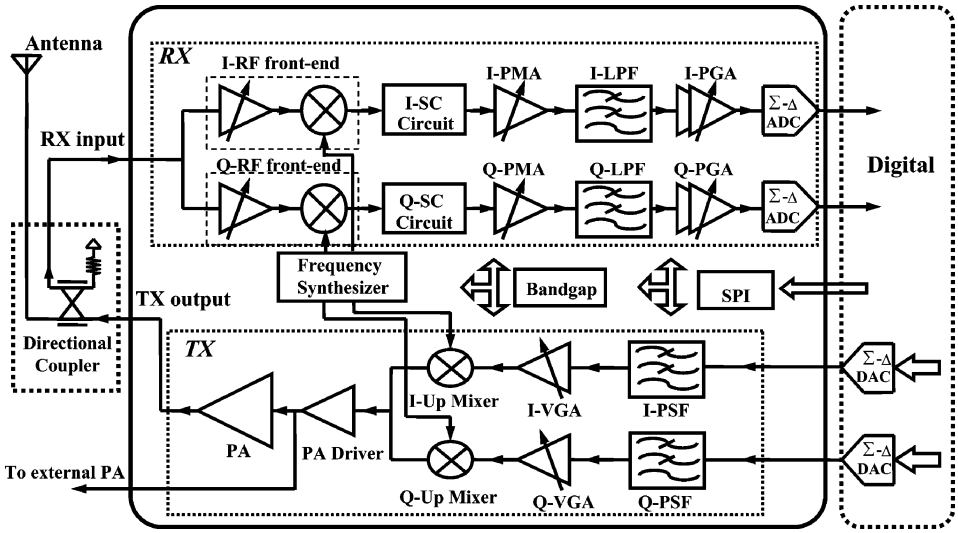


Fig. 2. The proposed chip architecture.

The noise floor (N_{floor}) can be expressed as

$$N_{\text{floor}} = \text{Sensitivity} - \text{SNR}_{\text{RX}} \tag{1}$$

where SNR_{RX} is the targeted SNR of the receiver. To avoid the impact on the sensitivity, the transmitter noise should be at least 3 dB smaller than the noise floor. Thus, the output SNR of the CW signal (SNR_{CW}) should satisfy the following relationship:

$$\begin{aligned} &P_{sj} - \text{SNR}_{\text{CW}} < N_{\text{floor}} - 3\,\text{dB} \\ &\quad \Rightarrow \text{SNR}_{\text{CW}} > P_{sj} - \text{Sensitivity} + \text{SNR}_{\text{RX}} + 3\,\text{dB} \end{aligned} \tag{2}$$

where P_{sj} is the self-jammer power.

If we assume the P_{sj} is -5 dBm, the targeted sensitivity is -80 dBm, and the targeted SNR_{RX} is 11.6 dB, the SNR_{CW} should be at least more than 89.6 dB. Therefore, the equivalent input magnitude of the CW signal from the digital block should be large enough to achieve a sufficient input SNR of the CW signal. Besides, it is better to adjust the magnitude of the CW signal in RF or analog domain not in digital domain to maintain the enough output SNR of the CW signal.

III. System Architecture and Specifications

The proposed system architecture is shown in Fig. 2. Both receiver and transmitter adopt the I/Q direct-conversion architecture.

The reader is designed for a single antenna sharing by the transmitter and receiver for high integration and low cost. A directional coupler is chosen for the isolation between the transmitter and receiver. It attenuates the self-jammer by 35 dB to relax the linearity requirements for the RF front-end, at the cost of 15 dB loss in sensitivity which is still acceptable for the system.

The receiver consists of the RF front-end, SC circuit, post-mixer amplifier (PMA) in parallel with the DCOC, low-pass filter (LPF), programmable gain amplifier (PGA) in parallel with the DCOC, and the sigma-delta ADC. In order to obtain a high $P_{1\text{dB}}$ with sufficient conversion gain and good noise performance, an active mixer using capacitor cross-coupled (CCC) common-gate stage as the input stage and vertical NPN BJT as the switching stage is adopted. After the mixer, both the self-jammer and the wanted signal are linearly amplified and down-converted to DC domain, the DC leakage is removed by the on-chip SC circuit with quickly time-varying cut-off frequency within a short time. The PMA, LPF, PGA and sigma-delta ADC are following the SC circuit. Two DCOC loops in parallel with the PMA and PGA are used for canceling the DC offset generated from the analog baseband, as well as further killing the residual of the DC leakage from the self-jammer within a short time.

The transmitter consists of the pulse-shaping filter (PSF), variable gain amplifier (VGA), up-conversion mixer, PA driver, and CMOS class-AB PA. The PSF is used for suppressing the quantization noise of the sigma-delta DAC in the outside band. The highly linear up-conversion mixer, the class-A PA driver, and the CMOS class-AB PA are implemented to meet the stringent spectrum mask.

Additionally, a sigma-delta fractional-N frequency synthesizer with a single *LC* VCO is used to cover dual bands of 840–845 MHz and 920–925 MHz and to achieve the accurate locking frequencies and quick channel hoping time. A bandgap and current reference circuit are used to provide several accurate reference voltages and reference current sources. A serial peripheral interface (SPI) is used for the communication between the inside chip and the external world.

The system specifications are taken into consideration as follows.

A. Linearity

The receiver RF front-end pays more attention to $P_{1\text{dB}}$ instead of IIP3, because the RF front-end should tolerate the large self-jammer without desensitizing the wanted signal. The output

signal amplitude of the fundamental frequency (A_o) behind the receiver RF front-end can be expressed as follows:

$$A_o = \left(\alpha_1 + \frac{3\alpha_3 A_{sj}^2}{2}\right) A_w \tag{3}$$

where A_{sj} and A_w are the amplitude of the self-jammer and the wanted signal, respectively. Since 1 dB compression point ($A_{1\mathrm{dB}}$) is defined as

$$\begin{aligned} 20\log\left(\frac{A_o}{A_w}\right) &= 20\log\left|\alpha_1 + \frac{3\alpha_3 A_{1\mathrm{dB}}^2}{4}\right| \\ &= 20\log|\alpha_1| - 1\,\mathrm{dB}. \end{aligned} \tag{4}$$

It indicates that the effect of desensitization by the self-jammer in (3) is similar to the effect of gain compression in (4), but they have different coefficients. Making (3) and (4) equal, we can get the equation as

$$\begin{aligned} \alpha_1 + \frac{3\alpha_3 A_{sj}^2}{2} &= \alpha_1 + \frac{3\alpha_3 A_{1\mathrm{dB}}^2}{4} \\ &\Rightarrow 20\log A_{1\mathrm{dB}} = 20\log A_{sj} + 3\,\mathrm{dB}. \end{aligned} \tag{5}$$

When the self-jammer A_{sj} is 3 dB smaller than $A_{1\mathrm{dB}}$, the output signal is just desensitized by 1 dB. Therefore, to give a margin of 3 dB, the $P_{1\mathrm{dB}}$ of the receiver should be 6 dB larger than the self-jammer to avoid blocking the wanted signal.

As we adopted the directional coupler with 35 dB isolation from transmitter to receiver, the $P_{1\mathrm{dB}}$ of the receiver RF front-end should be at least -9 dBm for 20 dBm transmitter power in mobile applications, and 1 dBm for 30 dBm transmitter power, respectively.

B. Sensitivity

The sensitivity theoretically depends on the noise figure (NF), the noise bandwidth (BW), and the minimum required signal-to-noise ratio ($\mathrm{SNR_{min}}$). Taking the receiver input port behind the directional coupler as the reference point, we can get the sensitivity expression as

$$\mathrm{Sensitivity} = -174 + 10\log\mathrm{BW} + \mathrm{NF} + \mathrm{SNR_{min}}. \tag{6}$$

BW is determined by the data rate, encoding and modulation schemes. The power spectrum of \FM 0 and Miller encoding has a non-DC characteristics and mainly has the signal bandwidth of about twice the link frequency (LF) [13]. Thus, the LPF for channel selection has a cut-off frequency of twice LF, while BW is four times of LF for zero-IF receiver. In our system, the cut-off frequency of the LPF is tunable from 80 to 640 kHz to cover the data rate from 40 to 320 kbps. Another key factor for the sensitivity is $\mathrm{SNR_{min}}$. For the targeted BER of 0.001%, the $\mathrm{SNR_{min}}$ is 11.6 dB for ASK \FM 0 coding [14]. After BW and $\mathrm{SNR_{min}}$ are specified, the good sensitivity depends on the small NF.

However, different from the other systems, the sensitivity of the reader receiver also highly depends on the linearity, which is actually characterized as the $P_{1\mathrm{dB}}$ of the RF front-end. Note that the sensitivity must include the loss of the directional coupler ($\mathrm{Loss_{coupler}}$), which has some positive correlation with the isolation ($\mathrm{Iso_{coupler}}$) as

$$\begin{aligned} \mathrm{Loss_{coupler}} = \alpha \cdot \mathrm{Iso_{coupler}},\ 0 < \alpha < 1, \\ \mathrm{Loss_{coupler}} > 0,\ \mathrm{Iso_{coupler}} > 0. \end{aligned} \tag{7}$$

Owing to the isolation of the coupler, the self-jammer power (P_{sj}) will be decreased from the transmitter power (P_{TX}) by $\mathrm{Iso_{coupler}}$ dB. As discussed above, P_{sj} should be 6 dB less than the $P_{1\mathrm{dB}}$, as expressed below:

$$P_{sj} = P_{\mathrm{TX}} - \mathrm{Iso_{coupler}} \le \mathrm{P_{1dB}} - 6\ \mathrm{dB}. \tag{8}$$

On account of (7) and (8), the sensitivity of the reader receiver should be revised to

$$\begin{aligned} \mathrm{Sensitivity} = -174 + 10\log\mathrm{BW} + \mathrm{NF} \\ +\mathrm{SNR_{min}} + \alpha(P_{\mathrm{TX}} - P_{1\mathrm{dB}} + 6\ \mathrm{dB}), 0 < \alpha < 1. \end{aligned} \tag{9}$$

Thus, the sensitivity can be improved by enhancing $P_{1\mathrm{dB}}$, since higher $P_{1\mathrm{dB}}$ implies that we can choose the coupler with smaller isolation, which correspondingly results in smaller loss.

However, higher $P_{1\mathrm{dB}}$ cannot guarantee a better sensitivity, due to the noise contribution of the analog baseband. To further clarify the sensitivity, (9) should be re-estimated as

$$\begin{aligned} \mathrm{Sensitivity} = &-174 + 10\log\mathrm{BW} + \mathrm{NF_{RF}} \\ &+ \frac{\mathrm{NF_{BB}} - 1}{G_{\mathrm{RF}}} + \mathrm{SNR_{min}} \\ &+ \alpha(P_{\mathrm{TX}} - P_{1\mathrm{dB}} + 6\ \mathrm{dB}),\ \alpha < 1, \\ G_{\mathrm{RF}} = &P_{\max} - P_{1\mathrm{dB}} + 6\ \mathrm{dB}. \end{aligned} \tag{10}$$

The G_{RF} is the available gain of the RF front-end, which is limited by the $P_{1\mathrm{dB}}$ and the maximum allowable output power ($P_{\max}$). The $\mathrm{NF_{RF}}$ and $\mathrm{NF_{BB}}$ are the noise figure of the RF front-end and the analog baseband, respectively.

If we only focus on high linearity, the passive mixer could be used. But it will suffer from a bad $\mathrm{NF_{RF}}$, and there will be no G_{RF} to suppress the noise from the analog baseband. Thus, it is necessary to make a good tradeoff between the $P_{1\mathrm{dB}}$ and the noise performance to achieve an optimum sensitivity. In this paper, a highly linear active mixer is able to tolerate the self-jammer. It also achieves good noise performance and sufficient voltage gain to suppress the noise from the analog baseband to achieve optimal sensitivity.

C. Phase Noise

The phase noise injected by the adjacent and alternative channel interference should be taken into account. Assuming that the interference from other reader transmitter is located at the adjacent or alternative channel, the power spectrum of such interference (P_i) must be below the noise floor (N_{floor}) to avoid flooding the wanted signal. With 3 dB margin, we get the following relationship:

$$P_i + \mathrm{ACPR}_i \le N_{\mathrm{floor}} - 3\,\mathrm{dB} \tag{11}$$

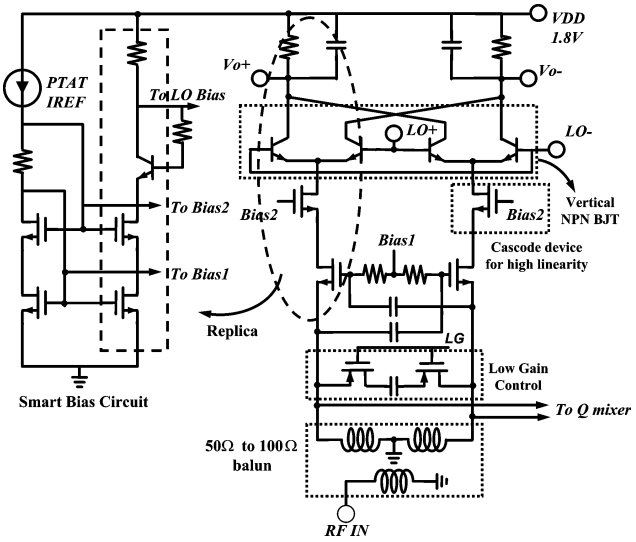


Fig. 3. Schematic of the mixer with the smart bias circuits in the receiver.

where ACPR_i is the adjacent or alternative channel power response. On the other hand, the phase noise injected by such interference should also be lower than N_{floor}, which is shown as

$$P_i + PN + 10\log \mathrm{BW} \leq N_{\mathrm{floor}} - 3\,\mathrm{dB} \tag{12}$$

where PN is the phase noise at 125 kHz or 375 kHz offset for the adjacent channel or the alternative channel, respectively. By combining (11) and (12), the phase noise has a relation as

$$PN \leq \mathrm{ACPR}_i - 10\log \mathrm{BW}. \tag{13}$$

As to the BW of 160 kHz for 40 kbps data rate, and on account of the spectrum mask in China, the phase noise are -92 dBc/Hz at 125 kHz offset and -112 dBc/Hz at 375 kHz offset.

D. Chinese Standard

In addition to the protocols of EPC class-1 generation-2 and ISO/IEC 18000–6C, this reader also meets the Chinese local standard [8]. The chip operates in dual bands of 840–845 MHz and 920–925 MHz with forty channels of 250 kHz bandwidth. The spectrum mask in China is required to be -40 dBc for ACPR_1, -60 dBc for ACPR_2, and -65 dBc for ACPR_3, respectively.

IV. Circuit Implementation

A. Receiver

1) RF Front-End: Because of the large self-jammer, there is no LNA in RF front-end, but an active mixer as illustrated in Fig. 3. Based on the capacitor cross-coupled (CCC) common-gate LNA topology in [15], we adopt the CCC common-gate stage as the input stage. Instead of using a tail current source, an external 50 Ω to 100 Ω balun is used to realize the impedance matching between the directional coupler and two I/Q mixers, and consequently improve the voltage headroom for the mixer. The common-gate input stage can provide a good wideband input matching from 840 MHz to 925 MHz. In contrast with the traditional common-gate stage, the CCC scheme can effectively improve the noise figure and get the same input matching with only half current consumption.

The existence of the large self-jammer requires a high $P_{1\mathrm{dB}}$. The Derivative Superposition method in [16] is widely used to improve the linearity. Nevertheless, it is much more sensitive to the PVT (process, voltage and temperature) variations, because it needs an auxiliary MOSFET working in subthreshold region to cancel out the second-derivative of the transconductance $(gm^{\|})$ of the main transistor. Instead, we utilize a cascode transistor between the transconductance stage and the switching stage to cancel out the $(gm^{\|})$ by properly choosing the bias voltage and the transistor size.

To ensure the high linearity regardless of the PVT variations, a smart bias circuit is designed as described in Fig. 3. The stacked devices in the mixer are replicated in proportion to the smart bias circuit, which is driven by a PTAT current source. If there are PVT variations, the bias voltages generated by the smart bias circuit will vary correspondingly, and then the current of the mixer will always check the PTAT current source. Compared to the fixed bias voltages, this method is smart and is able to maintain the stable performance without the PVT variations.

The flicker noise is another crucial problem for the direct-conversion receiver, especially for the narrow bandwidth system. As in [17], the parasitic vertical NPN BJTs are adopted as the switching stage to lower the flicker noise corner to less than 4 kHz. The vertical NPN BJTs with 5×5 μm emitter area in our deep N-well CMOS standard process has a transient frequency of about 2.3 GHz, and a current gain (β) of about 20, which are sufficient for the 900 MHz operation frequency in the reader system.

What is more, two gain modes are implemented to cope with the different self-jammer environment. In high gain mode, the mixer achieves 16 dB gain with -8 dBm $P_{1\mathrm{dB}}$ to deal with the self-jammer of -15 dBm , corresponding to the mobile applications with over 20 dBm transmitter power. By adding a capacitor in the input node to weaken the input matching, the mixer changes to the low gain mode of 7 dB gain, and achieves 0 dBm $P_{1\mathrm{dB}}$ for the larger self-jammer of -5 dBm, when the transmitter sends the larger output power up to 30 dBm.

2) SC Circuit: As illustrated in Fig. 4(a), the proposed SC circuit is connected with the mixer, and followed by the PMA. It is used for removing the DC leakage within a short time.

According to the principle of the AC-coupling scheme, such as in [4] and [6], the SC circuit adopts an equivalent *RC* high-pass filter with a time-varying cut-off frequency corner. The switches in the SC circuit are controlled by the sequential logic as shown in Fig. 4(b). The control signals are provided from the SPI, which is controlled by the external logic. Once the transmitter starts to send the CW signal, the "Parallel Switch" has closed and the "Serial Switch" is opened to form a higher cut-off frequency, resulting in killing the DC leakage and the wanted signal rapidly. Subsequently, the "Parallel Switch" changes to open and the "Serial Switch" is closed to achieve a near-zero cut-off frequency, so that it can pass the wanted signal without the DC leakage. Just due to such scheme of quickly time-varying cut-off frequency corner, the DC leakage can be

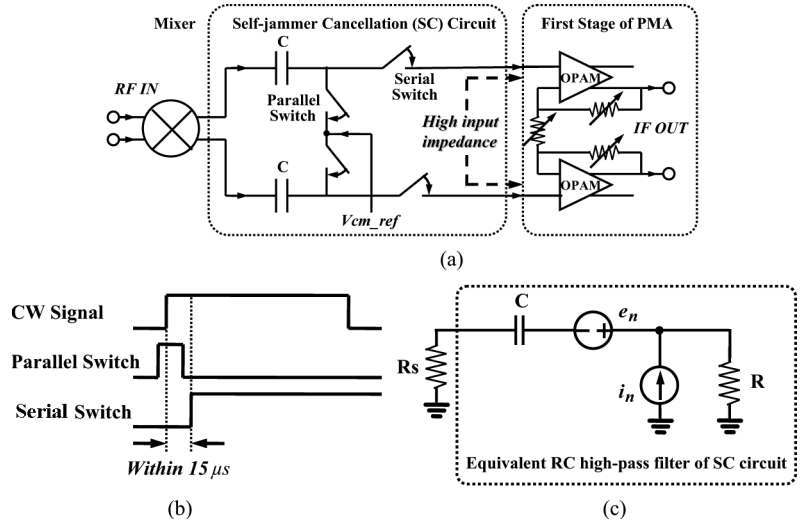


Fig. 4. (a) On-chip self-jammer cancellation (SC) circuit. (b) The sequential logic of the control signals. (c) The equivalent circuit for noise analysis.

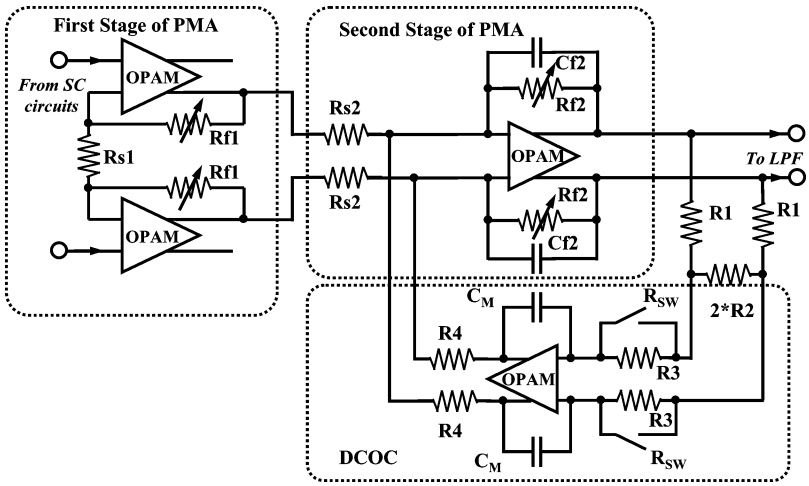


Fig. 5. Schematic of the PMA in parallel with the DCOC in the receiver.

cancelled rapidly within 15 μs, which meets the transmit-to-receive turn-around requirements [2]. The switches utilize the CMOS pairs with special width ratio to reduce the charge injection. Even if there is some residual injected charge which has not been compensated, the error voltage can be corrected by the following DCOC loop in parallel with the PMA.

Besides the functionality, the value of the resistors and capacitors will significantly affect the noise performance. As illustrated in Fig. 4(c), the noise current i_n generated by the shunt resistor R will introduce the noise voltage e_n, when the i_n flows through the AC-coupling capacitor C and the output resistance of the mixer (R_s). The noise voltage can be express as follows:

$$\begin{cases} \overline{e_n^2} = 4kT \cdot R_{n,eq} = 4kT \cdot \frac{R_s}{R} \cdot R_s, & \text{when } \left|\frac{1}{sC}\right| \ll R_s \\ \overline{e_n^2} = 4kT \cdot R_{n,eq} = 4kT \cdot \frac{f_c}{f} \cdot \left|\frac{1}{sC}\right|, & \text{when } \left|\frac{1}{sC}\right| \gg R_s \end{cases} \tag{14}$$

where f_c is the high-pass cut-off frequency of the SC circuit when it is stable, and R_s is the output resistance of the mixer.

According to (14), the noise can be ignored, when the C is very large and the R is over tens of times larger than R_s. Thus, the off-chip method by using the large off-chip capacitors in [4] and [6] will not deteriorate the noise performance. But unfortunately, it needs four off-chip capacitors and eight pins in the package for the I/Q architecture.

A potential option for the high integration is to utilize a smaller capacitor of several pF and a large resistor of several MΩ to construct the SC circuit, which is still feasible to be integrated on-chip. However, according to (14), it will lead to unacceptable large noise. Assuming the C is 10 pF, R is 3 Ω, and the f_c is 5 kHz or below, the equivalent noise resistance $R_{n,eq}$ is over 50 kΩ at 40 kHz. Hence, we cannot employ this solution to construct the on-chip SC circuit.

Fortunately, this paper proposed an on-chip SC circuit, as illustrated in Fig. 4(a). Because of the high load impedance provided by the following PMA, the on-chip capacitor of several pF can be used. The equivalent f_c of the SC circuit is close to zero, and the noise introduced by the SC circuit is negligible. Therefore, compared to the off-chip method in [4] and [6], this on-chip SC circuit successfully achieves high integration, good noise performance, and consumes small silicon area, which is valuable for the mobile applications.

3) PMA With DCOC: The analog baseband circuits are based on the general OPAM of two-stage Miller-compensated

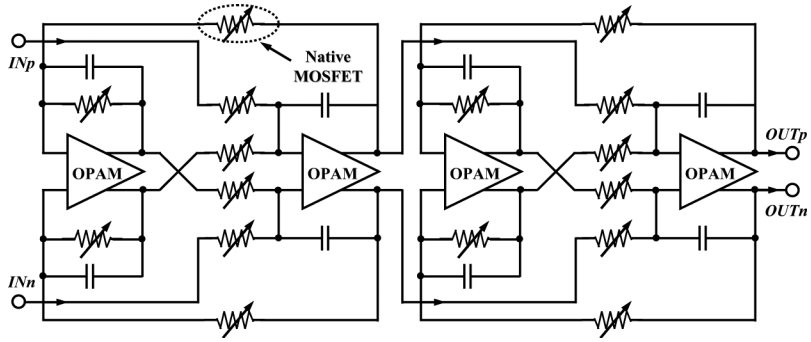


Fig. 6. Schematic of the LPF in the receiver.

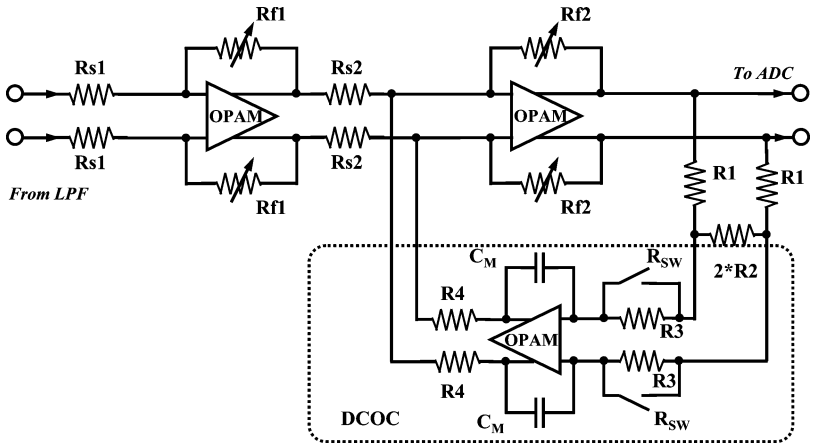


Fig. 7. Schematic of the PGA in parallel with the DCOC in the receiver.

and zero-nulling topology with low noise and small DC offset. As shown in Fig. 5, the PMA is used to suppress the noise from the analog baseband. It consists of two stages. The first stage, constructed by two OPAMs, provides high load impedance for the SC circuit, which makes the on-chip capacitors applicable in the SC circuit. The second stage is a resistor feedback close-loop amplifier based on a single OPAM. By adjusting the feedback resistors R_{f1} and R_{f2}, the PMA achieves the variable gain from 0 dB to 36 dB with 6 dB per step.

The DCOC loop is in parallel with the second stage of the PMA. It is used for correcting the DC offset from the PMA and the residual DC leakage after the SC circuit. It senses the DC offset at the output of the PMA, and compensates it at the input of the second stage. The equivalent high-pass cut-off frequency (f_{cutoff}) of the DCOC loop is expressed as

$$f_{\mathrm{cutoff}} = \frac{1}{2\pi} \cdot \frac{1}{(R_3 \| R_{\mathrm{SW}}) C_M} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{R_{f2}}{R_4}. \qquad (15)$$

The settling time of the DCOC is the reciprocal of f_{cutoff}. To avoid damaging the wanted signal, the f_{cutoff} should be lower than several kHz for all gain steps. Just since the resistor network of R_1 and R_2 divides the DC offset voltage, a small on-chip capacitor of several pF is feasible to realize the C_M. But the residual of the DC offset is in proportion to the ratio of $R_1 + R_2$ and R_2, which implies that we should make a good compromise between the small value of C_M and the small residuum of the DC offset.

A variable f_{cutoff} of the DCOC loop is realized by the switch R_{SW} in parallel with the R_3. When the SC circuit is killing the DC leakage, this R_{SW} is also closed to form a high f_{cutoff}, which corresponds to the short settling time and quickly kills the residual DC leakage. After the SC circuit converts to pass the wanted signal, this R_{SW} will still hold closed for several μs to further kill the residual DC leakage and stabilize the signals, and then change to be opened to form a low f_{cutoff}. On the collaboration of the SC circuit and the DCOC, the DC leakage can be cleanly cancelled within a short time.

4) LPF: To cover the LF from 40 kHz to 320 kHz, the LPF has a tunable cut-off frequency from 80 kHz to 640 kHz. As shown in Fig. 6, a fourth-order Bessel continuous-time low-pass filter with active MOSFET-C topology is chosen for the channel selection. The native MOSFETs working in deep linear region are adopted for the variable resistors to achieve good linearity. The tunable cut-off frequency is realized by adjusting the number of the series native MOSFETs. On the basis of the switched-capacitor technique in [18], an auto-tuning circuit provides the tuning voltage to control the gate of the native MOSFETs for accurate cut-off frequency.

5) PGA: As shown in Fig. 7, the PGA is a two-stage resistor feedback close-loop amplifier, which is digitally controlled to achieve 0 to 48 dB gain with 2 dB per step. A DCOC loop in parallel with the second stage of the PGA is used to cancel the DC offset generated by the LPF and the PGA.

6) ADC: The IF signal is digitized with a sigma-delta ADC. In contrast with other ADC topologies, such as the pipeline and flash architecture, it only needs one pin to connect the following digital circuits, which is beneficial for high integration and reducing the cost of the package. The ADC is a second-

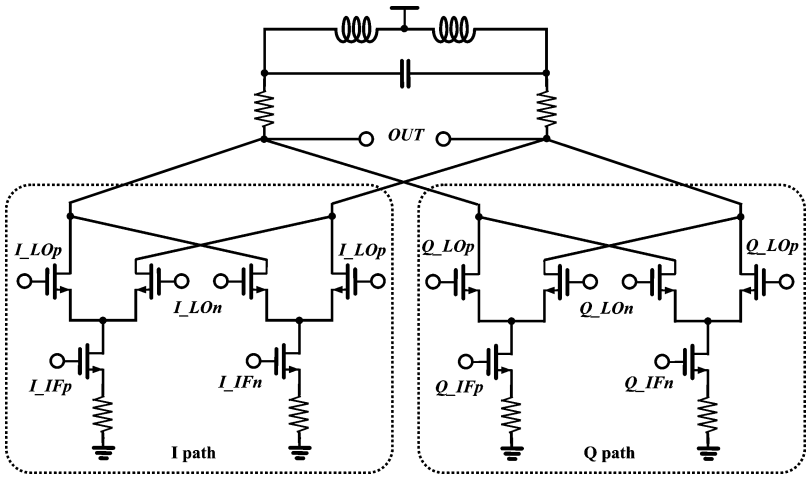


Fig. 8. Schematic of the up-conversion mixer in the transmitter.

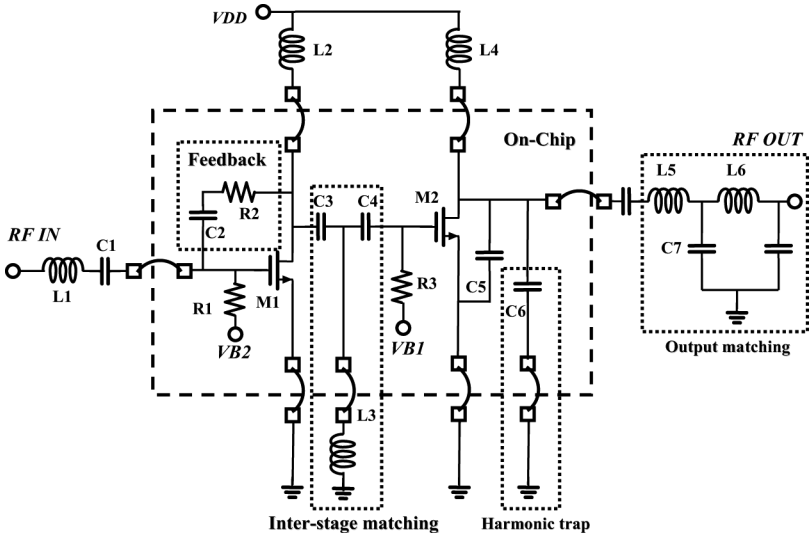


Fig. 9. Schematic of the CMOS PA in the transmitter.

order structure with two delaying discrete-time integrators and a two-level quantizer surrounded by two feedback loops. The frequency synthesizer provides the 32 MHz sampling clock, which is just twice the crystal reference frequency. The oversampling ratio (OSR) is 24 and the modulator has 50 dB dynamic range over the maximum signal bandwidth. The ADC consumes 0.2 mA current from the 1.8 V supply voltage.

B. Transmitter

To support the DSB/SSB-ASK and PR-ASK modulation, the transmitter also adopts the I/Q direct-conversion architecture. The digital signal from the sigma-delta modulator is reconstructed by the PSF. In front of the PSF, a limiter buffer is designed to limit the signal swing into the linear region of the PSF, and a single-to-differential converter is implemented to convert the signal to the differential-end signal. In addition, the PSF based on the fourth-order Bessel active LPF, is designed collaboratively with the digital blocks to suppress the quantization noise from the sigma-delta modulator. It shares the same auto-tuning circuit with the LPF in the receiver. The VGA following the PSF is also a resistor feedback close-loop amplifier, and the gain can be controlled by digital bits to adjust the transmitter power.

To meet the stringent spectrum mask of Chinese local requirements [8], a highly linear up-conversion mixer, a PA driver and a PA are implemented.

Fig. 8 shows the schematic of the up-conversion mixer. An artificially differential input stage with source degenerated resistor is adopted for the high linearity. I/Q mixers share the load network to sum the I/Q currents. A *LC* tank with a differential on-chip inductor is utilized to form a resonance at the middle frequency from 840 MHz to 925 MHz. A small series resistor is introduced to degenerate the quality factor of the *LC* tank, so that the frequency band of the resonance can be broadened to cover the PVT variations.

The class-A PA driver is implemented to drive the integrated PA for mobile applications or an external PA to deliver output power up to 30 dBm for longer communication distance.

Fig. 9 illustrates the class-AB CMOS PA. A two-stage topology is chosen to provide the sufficient power gain. Two L-type matching networks are cascaded for wideband output matching to cover from 0.8 GHz to 1 GHz. A series *LC* resonant path at the drain of the output transistor M2 shorts the second harmonic, and another 4 pF capacitor in parallel with M2 is used to shunt the higher order harmonics. Between the two stages, there is a pi-type matching network. In order to

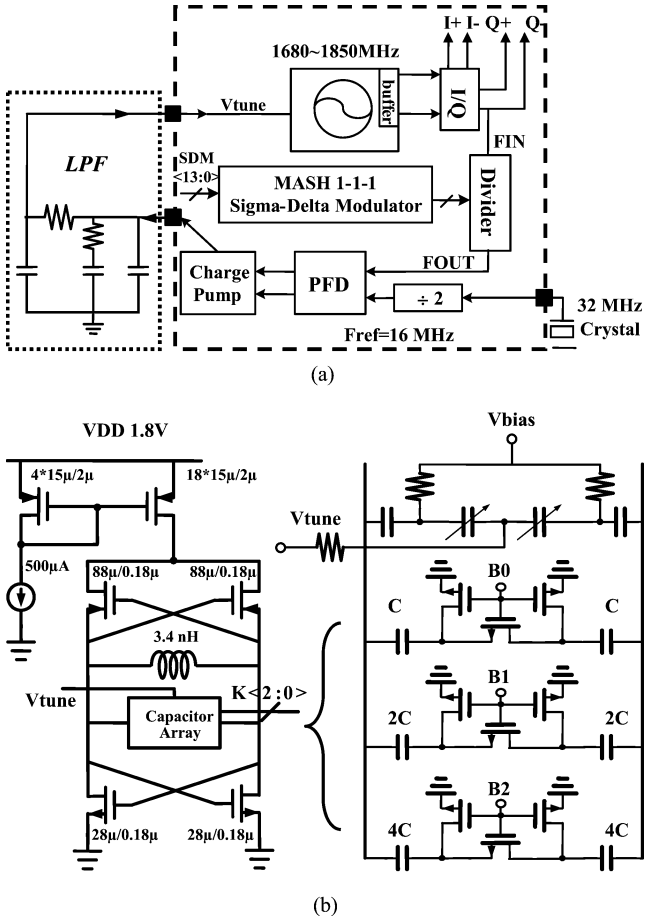


Fig. 10. (a) Architecture of the frequency synthesizer. (b) Schematic of the VCO.

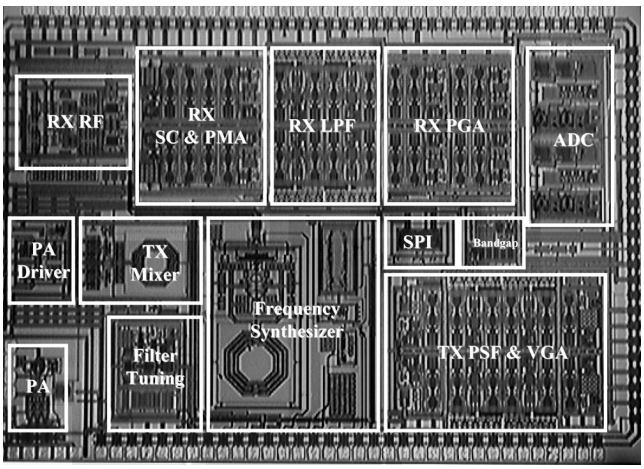


Fig. 11. Chip microphotograph of the UHF RFID reader transceiver.

guarantee the stabilization, a feedback network based on a 1 kΩ resistor in series with a 1 pF capacitor across the drain and gate of M1 is utilized. A proper gate voltage of M2 is optimized to achieve a high linearity. Some inductors are realized by the bonding wires. The PA is targeted at delivering the output power of over 20 dBm in linear region. The sufficient output power makes this PA feasible for the mobile applications, and it greatly enhances the integration and cuts down the cost of the reader system considerably.

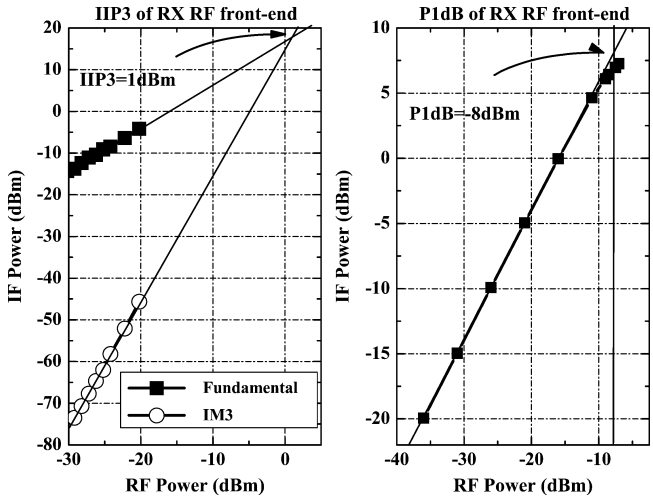


Fig. 12. Measured linearity of the receiver RF front-end.

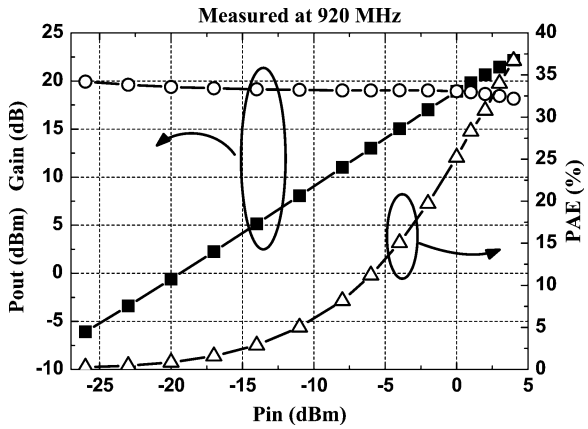


Fig. 13. Measured results of the PA in the transmitter.

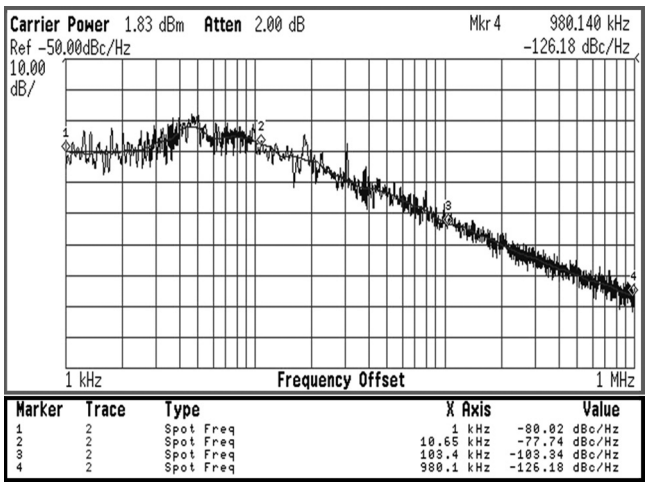


Fig. 14. Measured carrier phase noise of the transmitter output at 923.125 MHz.

C. Frequency Synthesizer

As depicted in Fig. 10(a), a fractional-N frequency synthesizer with a single *LC* VCO and a MASH 1-1-1 sigma-delta modulator (SDM) is integrated to cover the UHF RFID band in China with 250 kHz channel spacing. 16 MHz is chosen as

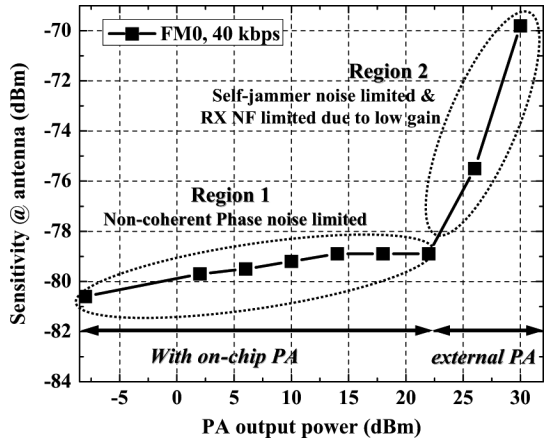
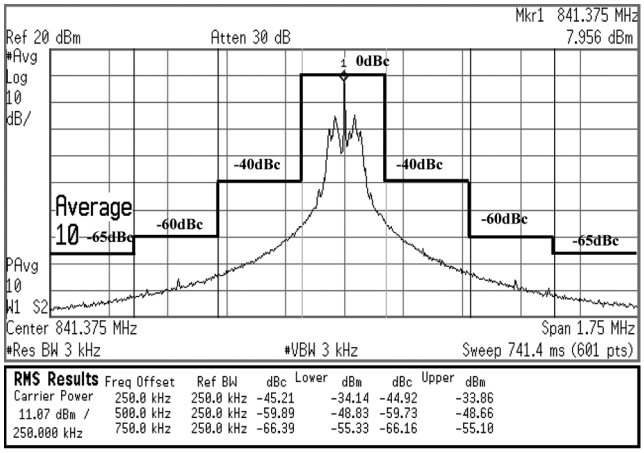
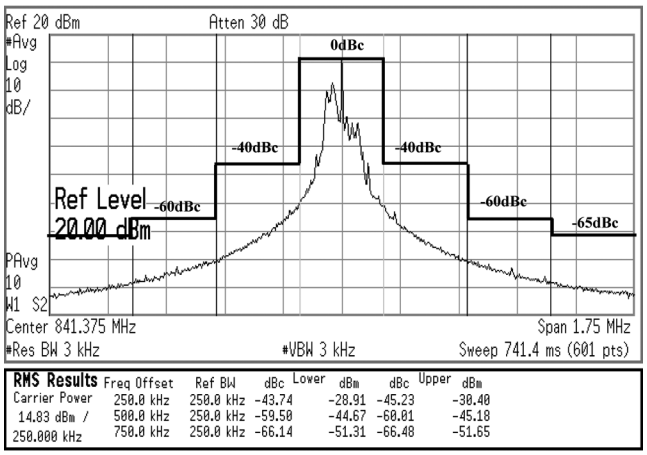


Fig. 15. Measured performance on sensitivity.



(a)



(b)

Fig. 16. Measured transmit spectrum of (a) DSB-ASK and Tari $= 25\ \mu$s and (b) SSB-ASK and Tari $= 25\ \mu$.

the reference frequency, because the center frequencies of the dual frequency bands of 840.125 to 844.875 MHz and 925.125 to 924.875 MHz would have the same fractional divide ratio, whereas the integer offsets are different. For instance, 840.125 divided by 16 equals to 52.5078125 and 920.125 divided by 16 is 57.5078125. Thus, the baseband algorithm can be simplified.

TABLE I
MEASURED PERFORMANCE SUMMARY

Receiver		
Sensitivity	-79 dBm [a] @ 22 dBm TX output	
RF front-end linearity @ high gain mode (16 dB)	P1dB	-8 dBm
	IIP3	1 dBm
RF front-end gain	16 dB to 7 dB	
Channel selectivity	80 kHz to 640 kHz	
Gain Range	7 dB to 100 dB	
Targeted Output SNR	11.6 dB	
Settling time of killing self-jammer	< 15 μs	
Output DC offset residuum	< 4 mV	
Transmitter		
PA driver	OP1dB	7.5 dBm
PA	OP1dB	19 dBm
	OIP3	24 dBm
	PAE @ 22 dBm	35 %
Spectrum mask	ACPR1	-45 dBc
	ACPR2	-60 dBc
	ACPR3	-66 dBc
Frequency Synthesizer		
Phase noise (VCO+PLL+TX)	@ 1 kHz offset	-80 dBc/Hz
	@ 100 kHz offset	-103 dBc/Hz
	@ 1 MHz offset	-126 dBc/Hz
Operating Frequency	840 – 845 MHz & 920 – 925 MHz	
Channel spacing	250 kHz	
Frequency Resolution	Within 2 kHz	
System		
Power	Without PA @ 7.5 dBm	203 mW
	With PA @ 22 dBm	660 mW
Supply Voltage	1.8 V and 3.3 V [b]	
Process technology	0.18 μm standard CMOS	
Die size	4.5 mm × 3.0 mm / 13.5 mm^2	
Package	8 mm × 8 mm 56-lead QFN	

[a] FM0 coding and 40 kbps data rate, including the 15 dB loss of the directional coupler
[b] 3.3 V supply voltage for the integrated CMOS PA

In addition, the interference from 16 MHz to analog baseband does not impair the wanted signal.

To reduce the area of the synthesizer, a multi-band VCO, which is able to cover the dual bands, is implemented as shown in Fig. 10(b). The VCO adopts NMOS/PMOS complementary cross-coupled transistors, which is easy to start the oscillation and consumes less current to achieve the same noise than other architectures. The VCO works at twice the required frequency and the balanced I/Q frequencies can be generated simply. Three digital bits are utilized to adjust the required frequency band.

As introduced in [19], a five-stage cascade divider chain consisting of 2/3 dividers is implemented as the programmable divider. It has several advantages, such as high speed, conformed units' structures and simple layout job, etc. There are five digital bits controlling the divider stages, where four of them are generated from the SDM and the most significant bit is assigned to 1. Thus, the five-stage divider chain is able to form any integer divide ratio from 48 to 63. In addition, the TSPC D-Latch is adopted in each 2/3 divider cell to guarantee high speed.

To achieve fractional-N dividing, a 14-bit MASH 1-1-1 SDM [20] is connected to the programmable divider to obtain a high frequency resolution within 1 kHz. High order SDM can push the noise to higher frequency so that it can be removed by the loop filter. To cooperate with the SDM, the bandwidth of the third-order loop filter is set to about 25 kHz to filter the SDM noise at higher frequency.

TABLE II
COMPARISON OF THE PUBLISHED SINGLE-CHIP UHF RFID READER TRANSCEIVERS

Reference	Ref [4] ISSCC 2007	Ref [5] ISSCC 2007	Ref [6] JSSC 2008	Ref [7] JSSC 2008	This work
Process	0.18 μm SiGe BiCMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Integration level	RF + Analog + Digital baseband	RF + Analog + Digital baseband	RF + Analog + Data Converters	RF + Analog + Data Converters	RF + Analog + Data Converters
Frequency	860 to 960 MHz	860 to 960 MHz	860 to 960 MHz	860 to 960 MHz	840 to 925 MHz
Phase noise	-116 dBc @ 200 kHz -144 @ 3.6 MHz	-87 dBc @ 100 kHz -120 dBc @ 1 MHz	-101 dBc @ 100 kHz -120 dBc @ 1 MHz	-110 dBc @ 200 kHz -127 dBc @ 1 MHz	-103 dBc @ 100 kHz -126 dBc @ 1 MHz
Front-end P1dB in RX	4 dBm in high gain mode; 11 dBm in low gain mode	8 dBm	-20 dBm in high gain mode; -8 dBm in low gain mode	3.5 dBm	-8 dBm in high gain mode; 1 dBm in low gain mode
Sensitivity @ FM0, 40 kbps, 1% PER	-83 dBm @ 0dBm self-jammer	-70 dBm @ 0 dBm self-jammer	-85 dBm @ -10 dBm self-jammer	-70 dBm @ -5 dBm self-jammer	-79 dBm @ 22 dBm PA output power
Sensitivity reference point	@ antenna	@ RX input, not including the 10 dB loss of the directional coupler	@ RX input, not including the loss of the directional coupler	@ antenna, dual antennas for TX and RX respectively	@ antenna, including the 15 dB loss of the directional coupler
Method of killing self-jammer	Off-chip capacitors, AC-coupling	On-chip, DCOC	Off-chip capacitors, AC-coupling	On-chip, Active trap	On-chip, AC-coupling & DCOC
TX output Power	20 dBm	4 dBm	10 dBm	10.4 dBm	22 dBm
Supply voltage	1.8 V, 3.3 V and 5 V	1.8 V	1.8 V	1.8 V	1.8 V and 3.3 V [a]
Power	1.5 W	160 mW	540 mW	<276.4 mW	203 mW w/o PA @ 7.5 dBm output; 660 mW w/ PA @ 22 dBm output
Die size	21 mm^2	23.9 mm^2	36 mm^2	18.3 mm^2	13.5 mm^2

[a] 3.3 V supply voltage for the integrated CMOS PA

V. MEASUREMENT RESULTS

This chip is fabricated in a standard 0.18 μm CMOS process. Fig. 11 is the die microphotograph of the single-chip UHF RFID reader transceiver, which occupies 4.5 mm $\times$ 3.0 mm silicon area, including the electrostatic discharge (ESD) I/O pads. It is housed in a 8×8 mm body 56-lead QFN package for good thermal properties and RF grounding. The layouts of the receiver RF front-end and the PA are placed at the corner of the chip to obtain the good RF grounding by bonding wire to the base plate of the QFN package. They are both placed at the same side of the chip to make the PCB connection between them and the directional coupler convenient. Besides the guard ring, the isolation ring with deep N-well is widely utilized to surround the PA and the noise-sensitive blocks. Based on the FR4 PCB board for testing and the FPGA for digital algorithm, the chip is measured as follows.

As shown in Fig. 12, the receiver RF front-end has a $P_{1\mathrm{dB}}$ of -8 dBm and IIP3 of 1 dBm, respectively, in the high gain mode with 16 dB gain. It is sufficient for the system specification when the transmitter sends a power of 20 dBm for mobile applications. The $P_{1\mathrm{dB}}$ is enhanced to 1 dBm in the low gain mode with 7 dB gain, which is used for tolerating the larger self-jammer when the transmitter delivers a power up to 30 dBm for longer communication distance. The two I/Q mixers consume 2.3 mA current from the 1.8 V supply voltage.

Fig. 13 illustrates the measured results of the PA. It has an $\mathrm{OP}_{1\mathrm{dB}}$ of 19 dBm, which means a good linearity to maintain the shape of the transmitter spectrum. It is able to deliver a large output power up to 22 dBm in linear mode with a PAE of 35%. The PA has the same good linearity in another frequency band of from 840 MHz to 845 MHz. This integrated PA enables the reader to save an external PA for mobile applications. If longer communication distance is needed, an external PA driven by the PA driver can be employed to deliver a power up to 30 dBm. The class-A PA driver has an $\mathrm{OP}_{1\mathrm{dB}}$ of 7.5 dBm in linear region.

Fig. 14 demonstrates the measured carrier phase noise of the transmitter output at 923.125 MHz, which is -103 dBc/Hz at 100 kHz offset and -126 dBc/Hz at 1 MHz offset, respectively. The phase noise includes the phase noise of VCO, PLL loop, and the transmitter, and it meets the requirements of the system specification. The phase noise is better at another frequency band from 840 MHz to 845 MHz due to the lower frequency. The measured frequency resolution is within 1 kHz for all 40 channels.

Fig. 15 illustrates the measured sensitivity performance versus the transmitter power level under \FM 0 encoding of 40 kbps data rate, when the channel selection bandwidth is 80 kHz and the targeted BER is 0.001%, corresponding to the SNR of 11.6 dB. Including the 15 dB loss of the directional coupler, the sensitivity is -79 dBm in the presence of the self-jammer, when the transmitter sends an output power of 22 dBm. As the output power becomes larger, the sensitivity degrades slightly, mainly attributed to the non-coherent phase noise generated from the slight nonlinear effect. It certifies that the phase noise is self-mixed to DC due to the single LO source, and the slight degradation of the sensitivity can be improved by adopting the transmitter output as the LO for the receiver. The sensitivity deteriorates drastically when the transmitter power is larger than 22 dBm by the external PA. It is mainly limited by the transmitter noise, and the degradation of the receiver noise figure, since the mixer is changed to low gain mode to reach

higher $P_{1\mathrm{dB}}$ to handle the larger self-jammer but be lack of suppressing the noise from the analog baseband. It is necessary to enhance the SNR of the transmitter CW signal to improve the sensitivity for the large transmitter power.

Fig. 16 describes the measured transmitter spectrum of DSB-ASK and SSB-ASK modulation at $\mathrm{Tari} = 25\ \mu\mathrm{s}$ with the integrated CMOS PA. Because the transmitter information is pulse-interval encoding (PIE) according to the EPC class-1 generation-2 protocol [2], there will be DC power in the spectrum. Thus, after the data is modulated to the RF carrier frequency, a pike will exist at the carrier frequency as shown in Fig. 16. The spectrum mask meets the Chinese standard [8], which is more stringent than the spectrum mask of the ETSI EN 302 208–1 [9] in Europe and the FCC Title 47, Part 15 [10] in the USA. The measured ACPR_1 is -45 dBc, the ACPR_2 is -60 dBc, and the ACPR_3 is -66 dBc for both DSB-ASK and SSB-ASK modulation.

From 1.8 V supply voltage, the transceiver consumes about 203 mW when delivering 7.5 dBm output power, and consumes about 660 mW when delivering about 22 dBm output power with the integrated PA (the PA is supplied from 3.3 V voltage), which is a low-power solution for the reader and consequently suitable for the handset terminals supplied by the battery.

Table I summarizes the measured performance of the single-chip UHF RFID reader transceiver, and Table II gives the comparison between the proposed UHF RFID reader transceiver with other published reader transceivers.

VI. Conclusion

A single-chip UHF RFID reader transceiver is implemented for the Chinese standard in a $0.18\ \mu$m standard CMOS process. The system considerations and the analysis on the system specification for the reader transceiver are presented. A highly linear mixer with $P_{1\mathrm{dB}}$ of -8 dBm in high gain mode of 16 dB gain is implemented to cope with the large self-jammer. The chip adopts the on-chip self-jammer cancellation (SC) circuit with rapidly time-varying cut-off frequency corner to kill the DC leakage within 15 μs, and the on-chip DCOC with quickly time-varying cut-off frequency corner is implemented to remove the residual DC leakage. The receiver achieves a sensitivity of -79 dBm in the presence of 22 dBm transmitter power. The integrated class-AB CMOS PA delivers up to 22 dBm power in the linear mode with 35% PAE. Besides the protocols of EPC class-1 generation-2 and ISO/IEC 18000-6C, the transceiver also meets the Chinese standard, and meets the more stringent spectrum mask, which is -40 dBc for ACPR_1, -60 dBc ACPR_2, and -65 dBc ACPR_3, respectively. The high integration of the CMOS PA and the on-chip method of removing the self-jammer, the low power of 203 mW, the low cost of the standard CMOS process, and the good sensitivity of -79 dBm, are beneficial for the mobile applications of UHF RFID reader.

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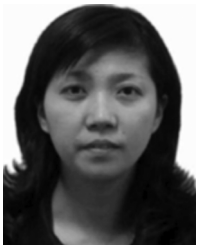

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