# Dual-Channel Pseudorandom Sequence Generator With Precise Time Delay Between Its Two Channels

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Abstract-In this paper, a dual-channel pseudorandom sequence generator is presented for the calibration of cross correlators in flow metering. In the sequence generator, the two channels have completely identical hardware structures so that they generate two identical sequences of pseudorandom signals to simulate two signals obtained from the upstream and downstream sensors of a cross correlator, respectively. Special control strategies in both hardware and software have been implemented in such a way that the error of time delay between the two channels can be reduced to less than a microsecond. The shift frequency and sequence length of each sequence channel and the time delay between the two channels can be adjusted in wide ranges to satisfy various requirements. The instrument has been evaluated by using a digital oscilloscope. Results obtained show that the control accuracy of time delay is equal to or better than 0.015% when the time delay is 1 ms or longer. Comparison with two commercially available noise signal generators shows that the error of time delay of the new generator is much smaller than those of the other two.

*Index Terms*—Calibration, control, cross correlator, microcontroller, pseudorandom sequence, shift register, signal generator, time delay.

## I. INTRODUCTION

SEUDORANDOM sequences [1] have been widely used in various fields, including communication, navigation, radar technology, cipher technology, remote control, measurement, and industrial automation. For instance, a pseudorandom sequence has been used in error-correcting codes [2], spread spectrum communication [3], and system identification and parameter measurement [4], [5]. Another example of application is found in surface characterization and 3-D scene modeling [6]. The design of a general-purpose pseudorandom sequence generator has matured and has already been commercialized [7]–[9]. However, a dual-channel pseudorandom sequence generator with precise control and adjustment of the time delay between its two channels has never been covered. In the development of cross-correlation-based flowmeters [10], such a dualchannel pseudorandom sequence generator was highly desired to calibrate and study cross correlators as well as algorithms.

In this paper, a novel design of a dual-channel pseudorandom sequence generator was presented to meet such a requirement. Two channels of pseudorandom sequences were generated by two hardware shift registers, and the shift frequency, sequence

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Digital Object Identifier 10.1109/TIM.2008.926427



Fig. 1. Principle of pseudorandom sequence generation.

length, and time delay between the two channels of sequences were fully controlled by an embedded microcontroller. The two channels of pseudorandom sequences were used to simulate signals obtained from the upstream and downstream sensors/transducers of a cross correlator. The time delay between the two channels of sequences determined the transition time of a random process from the upstream sensor to the downstream. In this design, the characteristic parameters of the instrument, i.e., the frequency of the shift clock, the sequence length of the sequence, and the time delay between the two channels, can be conveniently adjusted to meet the requirement of a wide range of applications.

### **II. PRINCIPLES**

#### A. Generation of Pseudorandom Sequence

A feedback shift register bank can be used to generate a pseudorandom binary sequence, which is, for simplicity, referred to as a pseudorandom sequence. The output of the shift register bank, which is either 0 or 1, is purely at random, whereas the sequence length and shift clock frequency (i.e., the bit rate) are both limited. In this sense, the sequence is pseudorandom. The generation of a pseudorandom sequence is schematically shown in Fig. 1. Such a generator consists of an n-tap shift register bank and a modulo-2 adder. If the initial states of the shift registers are not wholly zeroed, a pseudorandom sequence will be generated. Further, if the feedback bits are selected according to a certain criterion, an *m*-sequence can be obtained [1], [11]. An *m*-sequence is a pseudorandom sequence that has the longest period, i.e.,  $2^n - 1$ , for a given *n*-tap feedback shift register bank. In general, an *m*-sequence is preferred to make the best use of the shift registers. n is referred to as the sequence length and  $2^n - 1$  as the sequence period. Should the eigen-polynomial of the feedback circuit be primitive, this sequence has a statistical performance similar to white noise.

To change the sequence period, either the feedback logic or the sequence length should be varied. To meet practical requirements, five sequence lengths, namely, 11, 15, 17, 18, and 20, were selected in this research. The feedback points

Manuscript received November 8, 2006; revised April 17, 2008. First published June 24, 2008; current version published November 12, 2008.



Fig. 2. Simple implementation of the control of time delay between two channels of pseudorandom sequences.

were selected according to the primitive polynomials listed as follows [1]:

$$\begin{cases}
f_{11}(x) = 1 + x^{2} + x^{11} \\
f_{15}(x) = 1 + x + x^{15} \\
f_{17}(x) = 1 + x^{3} + x^{17} \\
f_{18}(x) = 1 + x^{7} + x^{18} \\
f_{20}(x) = 1 + x^{3} + x^{20}
\end{cases}$$
(1)

where the subscript of f denotes the sequence length, and the superscript of x denotes the bit number of the feedback point in the shift register bank.

The shift clock frequency can be varied to satisfy a practical requirement on the bandwidth of a pseudorandom sequence.

## *B. Implementation of Precise Control of Time Delay—Hardware Design*

A simple implementation of the control of the time delay between two channels of pseudorandom sequences is schematically shown in Fig. 2. Provided the two shift register banks for channels A and B have identical structures and the same initial state, a time delay  $\tau$  between the two channels can be achieved by enabling the second channel (channel B) after the first (channel A) has been enabled for a time period of  $\tau$ . However, the time delay obtained in this way is an integer multiple of the shift clock cycle, and the error could be as large as one cycle of the shift clock  $T_a$ . If the cycle of the shift clock is large, the error of obtained time delay could be identically large as well.

To reduce the error in the control of time delay, a frequency multiplicator can be applied to the shift clock to obtain a higher frequency clock that has a smaller cycle. Subsequently, a frequency divider is used to convert the clock back to the initial shift clock. The pseudorandom sequence is then started by enabling the corresponding frequency divider, as shown in Fig. 3. The feedback shift register is kept enabled, while the control of "enable/disable" is left to the frequency divider. In this case, the control error of time delay is, at most, as large as one cycle of the higher frequency clock  $T_b$ , which can be as small as required. In practical applications, the frequency multiplicator can be saved as a precise crystal oscillator can be used as a source of the high-frequency clock. The required shift clock is obtained by passing the oscillator clock through a suitable frequency divider (refer to Fig. 4).



Fig. 3. New implementation of the control of time delay between two channels of pseudorandom sequences.



Fig. 4. Generation of a pseudorandom sequence.

## **III. GENERATOR DESIGN**

The generator consists of a dual-channel pseudorandom sequence generating unit and a microcontroller unit, including corresponding software.

### A. Pseudorandom Sequence Generating Unit

A block diagram of the pseudorandom sequence generator is shown in Fig. 4. As the two channels have identical hardware structures, only one channel is presented.  $C_1$  to  $C_4$  are control signals generated by the microcontroller. As a 6-MHz crystal oscillator is used by the microcontroller, the oscillator clock is also used as the high-frequency clock.  $C_1$  is used to enable/disable the frequency divider and to start/stop the shift clock. The frequency-dividing depth is decided by the frequency-dividing control circuit that is further controlled by  $C_2$ . The shift register bank has 20 taps with a serial input and 20 parallel outputs. The sequence length selection circuit, under the control of  $C_4$ , decides which bits of the register bank are fed back to the exclusive OR (XOR) gate. The sequence length selection circuit is designed in terms of the primitive polynomials shown in (1).  $C_3$  is used to preset the shift registers with the required initial state. Identical initial states shared by the two channels is essential to guarantee the similarity of the two pseudorandom sequences. The initial state register was preset with a 20-bit initial state (i.e., 1100 0000 0000 0000 0000).

## B. Microcontroller Unit

The microcontroller unit is schematically shown in Fig. 5. The CPU is a single-chip microcontroller Intel 8031. The oscillator is a 6-MHz crystal precision oscillator. Light-emitting diodes (LEDs) are used to display the parameters and results. The keyboard is used to input the length and the time delay between the two channels.  $C_{1A}$  and  $C_{1B}$  are the start/stop commands for the two channels, respectively, and  $C_2$ ,  $C_3$ , and



Fig. 5. Schematic diagram of the microcontroller unit.

 $C_4$  are the common control instructions shared by the two channels, as defined before. The supervisory timer is used as a watch dog to guarantee a safe reset when the software runs out of control.

The monitoring software is written in MASM-51 and includes the following logical steps.

- On start up, read default constants from erasable programmable read-only memory (EPROM), and write to RAM. Otherwise, read constants from RAM.
- 2) Output commands  $C_3$ ,  $C_2$ , and  $C_4$ .
- 3) Generate START command signal  $C_{1A}$  for channel A.
- 4) Start the inner timer  $T_1$  with a time constant determined by the required time delay  $\tau$ .
- 5) Interrupt requested from timer  $T_1$ ? If yes, continue. If no, wait.
- 6) Generate START command signal  $C_{1B}$  for channel B.
- 7) Is any key pressed? If no, wait. If yes, continue.
- 8) Change constants, and return to step 1).

The microcontroller is used to start/stop the two channels at required time points to guarantee a precise time delay. Both sequences will not be changed until a parameter is adjusted, and a new command is generated.

## C. Implementation of Precise Control of Time Delay in Software

Apart from being used as a separate pseudorandom sequence generator, this generator is primarily used as an instrument for calibrating cross correlators. To this end, the control accuracy of time delay between the two channels  $\tau$  is of great importance. The error of time delay primarily comes from the following four aspects.

The first, i.e.,  $E_1$ , is the error due to the waiting time of the shift register whose flip-flop operations must be synchronous to a rising edge ("0" to "1" jump) of the shift clock. For a 6-MHz oscillator,  $E_1$  could be between 0 and 0.167  $\mu$ s.

The second, i.e.,  $E_2$ , is the error that stems from the limited resolution of the inner timer of Intel 8031. In fact, the time delay must be digitized into a timer constant that must be an integer multiple of the inner machine period. When a 6-MHz oscillator is used, the inner machine period is 2  $\mu$ s, and the error is between 0 and 2  $\mu$ s [13]. If the time delay is an integer multiple of the inner machine period,  $E_2 = 0$ .

The third term, i.e.,  $E_3$ , is the latency of the CPU response to a timer interrupt request. An 8031 takes three to eight inner machine periods to get to the interrupt routine, depending on the current instruction and the current register set. If the structure of

 TABLE I

 Sequence Period Versus Sequence Length and Shift Frequency

Sequence period in seconds		Shift frequency (Hz)					
		1465	732	366	183	92	
Sequence length (n)	11	1.40	2.80	5.59	11.18	22.37	
	15	22.37	44.74	89.48	179.0	357.9	
	17	89.48	179.0	357.9	715.8	1432	
	18	179.0	357.9	715.8	1432	2863	
	20	715.8	1432	2863	5727	11453	



Fig. 6. Example of two channels of pseudorandom sequences.

TABLE II List of Sample Rates

Time delay	20 µs - 30 ms	31 - 300 ms	301-1000 ms
Sample rate	100 MSamples/s	10 MSamples/s	1 MSamples/s
Time resolution	$0.01 \ \mu s$	$0.1 \ \mu s$	1 <i>µs</i>

the software is fixed and the instruction before a timer interrupt "REQUEST" is known in advance, the latency time can be obtained and compensated by deducting the corresponding number of inner machine periods from the timer constant. In the software designed by the authors, the instruction being executed is a Compare and Jump if Not Equal (CJNE) instruction (loop jump) that requires 4  $\mu$ s to execute. As a timer interrupt may be generated during the execution of the "loop jump," the latency of the CPU response to the timer interrupt request is between 0 and 4  $\mu$ s.

The fourth error, i.e.,  $E_4$ , is caused by the instructions in the interrupt service routine before the generation of the "start" command for the second channel. Once the software is designed, the time taken by executing these instructions can be similarly compensated by deducting an appropriate value from the timer constant.

In sum, the error of time delay between the two channels is

$$E = E_1 + E_2 + E_3 + E_4. \tag{2}$$

The relative error is noted by

$$e = E/\tau. \tag{3}$$

In fact, the generation of a timer interrupt is synchronized by the inner machine clock of the CPU. When the CPU is running a CJNE instruction, the latency time caused by executing this instruction can only be 0, 2, or 4  $\mu$ s if a timer interrupt is generated. Therefore, it is possible to add a suitable number of no-operation instructions (one inner machine period) so that the deduction from the timer constant made to compensate

TABLE III Measured Time Delays, as Compared With the Given Values (From 20 to 900  $\mu$ s)

Given (µs)	20	22	24	26	30	40	100	450	900
Measured( $\mu s$ )	20.15	24.15	24.15	28.15	32.15	40.15	100.15	452.15	900.15

TABLE IV Measured Time Delays, as Compared With the Given Values (From 1 to 1000 ms)

Given (ms)	1	2	5	30	31	100	500	1000
Measured (ms)	1.00015	2.00015	5.00015	30.00015	31.0002	100.0002	500.000	1000.000
Relative error (%)	0.015	0.008	0.003	0.001	0.001	0.000	0.000	0.000

 $E_3 + E_4$  is an integer multiple of two inner machine periods, i.e., 4  $\mu$ s. As a result, if we further select the time delay as an integer multiple of 4  $\mu$ s,  $E_2 + E_3 + E_4$  can be fully compensated. In this case, the absolute error is at most 0.167  $\mu$ s, and the relative error is, at most, 0.017% if the time delay is not less than 1 ms.

#### D. Operation Parameters

In the current design, the shift clock can be selected from 1465, 732, 366, 183, and 92 Hz. The sequence length of the pseudorandom sequence can be set to 11, 15, 17, 18, and 20, although any length between 2 and 20 is available. The time delay  $\tau$  can be set between 0 and 9999 ms. The sequence periods under various sequence lengths and shift frequencies are listed in Table I, where the sequence period has been converted to the corresponding time T. It is obvious that the sequence period can be selected in a wide-enough range and can meet majority of the practical requirements.

The operation parameters mentioned above were designed to calibrate and study cross correlators in flow metering. It should be noted, however, that the parameters of the generator could be adjusted in wider ranges by appropriate designs in hardware and software.

## **IV. EXPERIMENTAL RESULTS AND DISCUSSION**

An example of two channels of pseudorandom sequences is given in Fig. 6. The shift frequency, the sequence length, and the time delay were 732 Hz, 18, and 20 ms, respectively. It appears that the two channels of sequences share an identical waveform.

To study the control accuracy of the time delay between the two channels, a digital oscilloscope was used to digitize the two pseudorandom sequences. The data were fed into a personal computer via a general-purpose interface bus port to analyze the time delay between the two sequences. A number of points of time delay from 20  $\mu$ s to 1000 ms were tested. As the time resolution of the timer in the CPU is 2  $\mu$ s, only multiples of 2  $\mu$ s were tested. The sample length was 4000000 points. The sample rate varied with the time delay,<sup>1</sup> as given in Table II.





Fig. 7. Comparison of the relative error for the time delay of this generator with an E + H noise generator and an MP noise generator (time delay is 10–100 ms).

When the shift frequency and the sequence length are 732 Hz and 18, the measured time delays, as compared with the given values, are shown in Tables III and IV.

As the software and the timer constant were optimized for integer multiples of 4  $\mu$ s, the timer interrupt is always generated at the middle of the execution of the CJNE instruction if a time delay of a noninteger multiple of 4  $\mu$ s is tested. In this case, a further 2  $\mu$ s must expire before the instruction is completed. It can be seen from the test results for time delays from 20  $\mu$ s to 30 ms, as shown in Tables III and IV, that the absolute error of time delay was 0.15  $\mu$ s, which is between 0 and 0.167  $\mu$ s for integer multiples of 4  $\mu$ s and is 2.15  $\mu$ s for noninteger multiples of 4  $\mu$ s. The results are coincident with the analysis made in Section III. No effect was found, from the shift frequency and the sequence length, on the control accuracy of the time delay.

As the instrument is for calibrating cross correlators in flow measurement, a time delay that ranges between 1 and 1000 ms and a step size of 1 ms are adequate. Although 1 ms is an integer multiple of 4  $\mu$ s, the absolute error of time delay should be 0.15  $\mu$ s, as validated by the experimental results shown in Table IV, although the error cannot be fully differentiated by the oscilloscope when the time delay is larger than 30 ms. The relative error of the measured time delay to the given value is also shown in Table IV.

To evaluate the signal generator, the data of the commercial noise signal generator from Endress and Hauser (simplified as E + H) and the MP noise generator provided in



Fig. 8. Comparison of the relative error for the time delay of this generator with an E + H noise generator and an MP noise generator (time delay is 100–1000 ms).

[12] are compared with those of this generator in Figs. 7 and 8. It can be seen that the measurement error for time delay of the new generator is much smaller than that of the other two.

## V. CONCLUSION

A dual-channel pseudorandom sequence generator with precise control of the time delay between the two channels was developed for the calibration of cross correlators in flow measurement. Special control strategies implemented in both hardware and software were validated by experiments to be effective in decreasing the error of time delay between the two channels of pseudorandom sequences. For test points of time delay on integer multiples of 4  $\mu$ s, the absolute error was 0.15  $\mu$ s. When the time delay was not smaller than 1 ms, the relative error was smaller than 0.015%. For test points of time delay other than integer multiples of 4  $\mu$ s, the absolute error of time delay was 2.15  $\mu$ s. Comparison with an E + H commercial noise signal generator and an MP noise generator in the range of 10-1000 ms showed that the new generator was much better than the other two. The control accuracy of the time delay of the presented generator can meet the requirement of calibrating cross correlators for flow metering.

Moreover, the shift frequency, sequence length, and time delay can be easily adapted to a special application by a suitable redesign on the hardware and/or software.

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