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# Novel single-loop multi-bit sigma-delta modulator using OTA sharing technique without DEM

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**Abstract:** This paper presents a novel technique to shape feedback DAC mismatch without any extra digital elements inside the sigma-delta loop by inserting an analog integrator and an out-of-loop digital differentiator. To lower power dissipation, a novel triple integrator with low capacitor mismatch sensitivity of the delay paths is proposed. As a result, the SDM with three integrators is realized by only one OTA. The proposed topology, simulated at transistor level on 0.13 $\mu$m CMOS process, achieves 98.4 dB SNDR with 100 kHz bandwidth and 1.2 mW power dissipation from a single 1.2 V supply voltage. Its specification satisfies the GSM requirements.

**Keywords:** data converter, sigma-delta modulator, DAC mismatch shaping, amplifier sharing, GSM

**Classification:** Integrated circuits

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## 1 Introduction

Multi-bit sigma-delta modulators (SDMs) have become popular in communication systems in virtue of their lower quantization noise and higher stability, however, the issue of feedback DAC nonlinearity limits their performance. Dynamic element matching (DEM) [1] especially the data-weighed averaging algorithm (DWA) is the most widely used method to calibrate this error. Since for low-pass SDMs DWA mismatch shaping function of DAC error is $(1 - z^{-1})$ which is a first-order shaping [2], it can also be realized in analog domain [3] at the cost of an extra digital integrator (accumulator) inserted in SDM loop. Although the accumulator presents smaller feedback logic delay than DWA, the more bits of the DAC, the larger delay will appear. Furthermore, the mismatch between single-bit and multi-bit DACs of the accumulator limits the input level of the overall SDM.

In this paper, a novel feedback DAC mismatch shaping structure is proposed. Here, there is no digital elements appeared in the branches of feedback DACs, thus, the feedback logic delay will be avoided totally. Moreover, to reduce power consumption, a method to save the amounts of OTAs (operational transconductance amplifiers) is put forward. Finally, the proposed circuit was simulated under smic 0.13 $\mu$m CMOS technology.

## 2 Proposed DAC mismatch shaping structure

Without loss of generality, the idea of this work is presented by a standard $2^{nd}$-order 4-bit CRFB SDM [4] targeted for GSM applications which require 80-90 dB dynamic range (DR) and 100 kHz signal bandwidth. The coefficients of the SDM can be obtained by the Matlab toolbox [4] with 128 times oversampling rate (OSR) and 3.5 times maximum out-of-band gain noise transfer function.

The proposed topology is shown in Fig. 1 (a). Here, analog differentiators are inserted in the paths of DACs as [3], however, instead of using digital accumulators, an analog integrator is employed in the loop filter, and meanwhile, a digital differentiator is used before the output of SDM. Since the digital differentiator is out of the sigma-delta loop, it will not cause any delay in the SDM loop. And moreover, compared to the accumulator which has to deal with overflow, its implementation only needs simple digital delay and subtraction. The output of the overall SDM can be written as:

$$V = STF \cdot U + NTF \cdot Eq + MTF_1 \cdot Ed_1 + MTF_2 \cdot Ed_2, \quad (1)$$

where STF, NTF, $\mathrm{MTF}_1$ and $\mathrm{MTF}_2$ stand for the transfer function of the input U, quantization noise Eq, $1^{st}$ DAC mismatch $\mathrm{Ed}_1$ and $2^{nd}$ DAC mismatch $\mathrm{Ed}_2$, respectively. By calculating using linear model, we can obtain:

$$STF(z) = bc_1c_2 \cdot z^{-1}/D(z) \quad (2)$$

$$NTF(z) = (1 + (c_1g - 3) \cdot z^{-1} + (3 - c_1g) \cdot z^{-2} - z^{-3})/D(z) \quad (3)$$

$$MTF_1(z) = -a_1c_1c_2 \cdot z^{-1}(1 - z^{-1})/D(z) \quad (4)$$

$$MTF_2(z) = -a_2c_2 \cdot z^{-1}(1 - z^{-1})^2/D(z), \quad (5)$$


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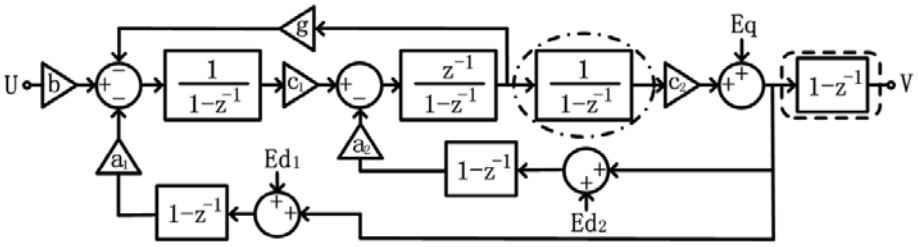
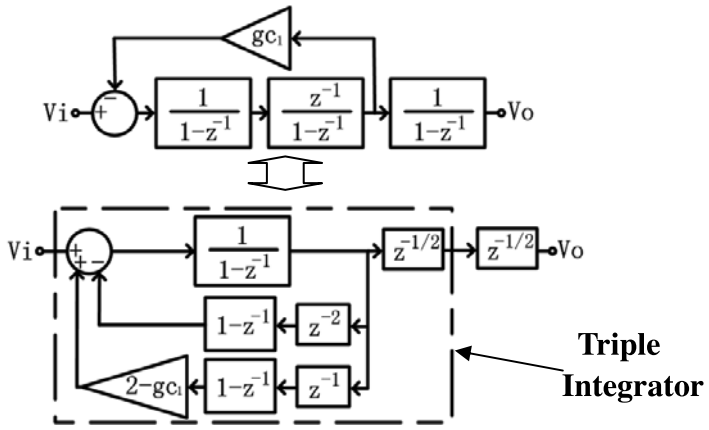
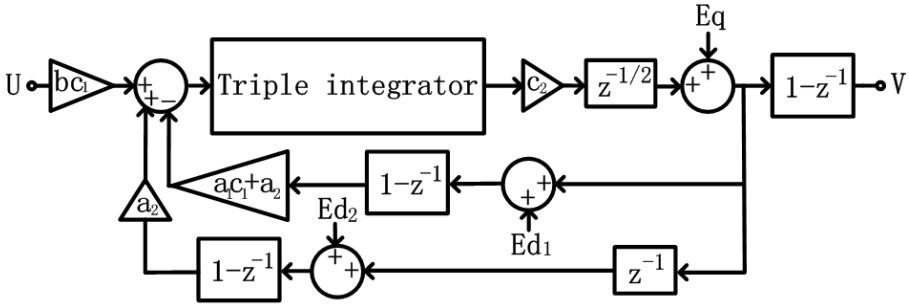


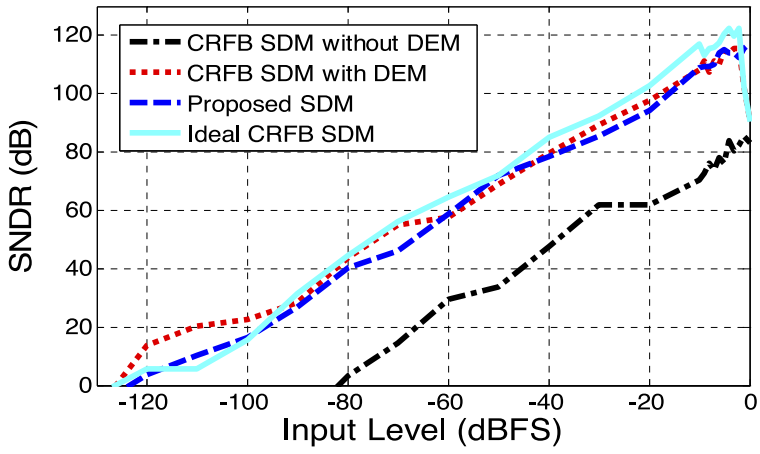

(a)




(b)




(c)




(d)

**Fig. 1.** Block diagrams of (a) proposed SDM, (b) proposed triple integrator, and (c) achieved SDM; (d) SNDR vs. input level for behavior simulation comparison of DAC elements mismatch.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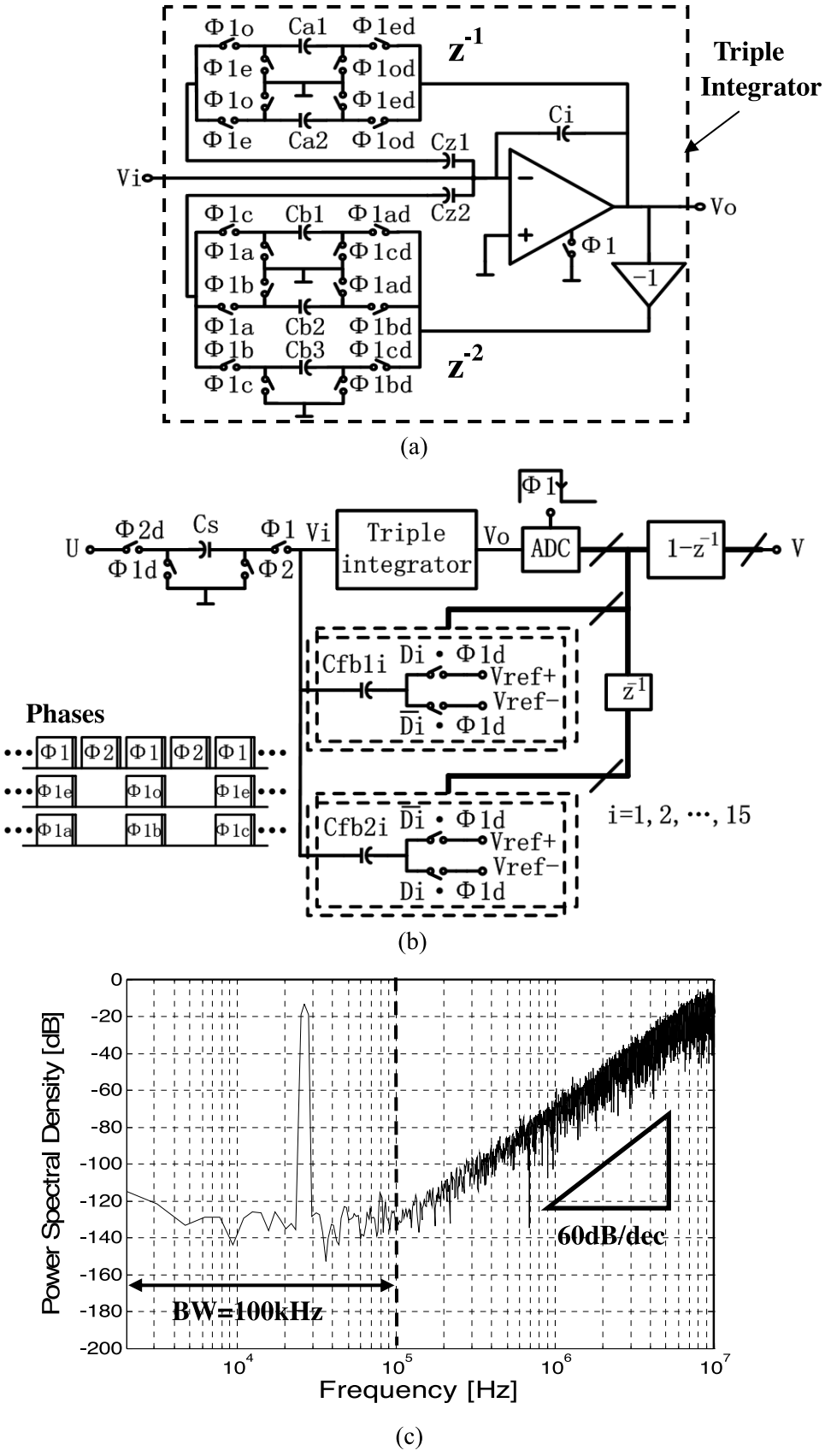


**Fig. 2.** Circuit implementations of (a) proposed triple integrator and (b) final switched-capacitor SDM (single-ended circuit for simplification, fully differential for actual design); (c) simulated output spectrum at transistor level.


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where $D(z) = 1 + (a_1c_1c_2 + a_2c_2 + c_1g - 2) \cdot z^{-1} + (1 - a_2c_2) \cdot z^{-2}$

Compared with a standard 2nd-order CRFB SDM, the denominator polynomial D(z) and STF(z) are unchanged, while, the NTF(z), $MTF_1(z)$ and $MTF_2(z)$ all have a 1st-order noise shaping enhanced. Hence, in the proposed structure, all the DAC mismatches can be shaped at least 1st order, and at the same time, the ability of quantization noise shaping of the overall SDM can also been enhanced.

## 3 Proposed technique for reducing the number of OTAs

In order for reducing power consumption caused by the extra analog integrator, an OTA sharing technique which realizes there integrators in series by only one OTA is proposed. As shown in Fig. 1 (b), the overall transfer function of the resonator and integrator can be presented as:

$$\frac{Vo(z)}{Vi(z)} = \frac{z^{-1}}{(1 - z^{-1}) - (2 - gc_1) \cdot z^{-1} \cdot (1 - z^{-1}) + z^{-2} \cdot (1 - z^{-1})} \quad (6)$$

After signal flow graph (SGF) manipulations, the final triple integrator with internal negative feedback path can be produced and shown in the bottom figure of Fig. 1 (b). Here, a half-cycle delay is extracted for the following quantizer. Its circuit structure is displayed in Fig. 2 (a). Capacitors with series switch are used to realize the $(1 - z^{-1})$ term and the blocks as [5] are used as delay operations. Here, the delay capacitors $C_{a1}$, $C_{a2}$ ($C_{b1}$, $C_{b2}$, $C_{b3}$) only work for sampling the output voltage and transfer it as the voltage of capacitor $C_{z1}$ ($C_{z2}$) unlike the capacitor mismatch sensitive circuits [5] where the delay capacitors are used directly as input capacitors. Thus, the gain of $(1 - z^{-1})$ paths totally depends on the ratio of input $C_{z1}$ ($C_{z2}$) and feedback capacitor $C_i$. Since the values of delay capacitors are not vital, there is little issue of mismatch among themselves or between the input capacitor and them. Circuit level simulations verified the case. Considering KT/C noise limit and power consumption, a 150 fF unity capacitor $C_U$ is used, and all the delay capacitors are $C_U$, while $C_i$, $C_{z2}$ are both 40 $C_U$ and $C_{z1}$ is realized by 79 $C_U$ with a 147 fF capacitor in parallel. Since delay capacitors are small, they have only a little influence on the output load capacitor of integrator.

## 4 Proposed topology

Using the proposed triple integrator and a series of SGF transformations, the final topology is shown in Fig. 1 (c). Dynamic-range scalings are performed to reduce output swing of the integrator and several simple adjustments of coefficients including rational approximations are also done to increase the maximum input signal level and convenience for the following circuit design. A behavior simulation using Matlab & Simulink is carried out to compare the proposed DAC mismatch shaping technique with generalized DWA, under 1% DAC random mismatches. As shown in Fig. 1 (d), without any DAC mismatch calibrating, the peak signal to noise and distortion ratio (SNDR)


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of a traditional CRFB SDM reduces 37 dB, while this work provides almost equal 6 dB drop as DEM. The circuits of the proposed SDM are shown in Fig. 2 (b), the quantizer is a 4-bit Flash ADC which reference voltage has a 0.5 times scaling to realize the 2 times gain of the quantizer's input path. The two branches of feedback DACs are realized by capacitors with series switch as [3]. The integrating operation is performed in phase $\Phi_1$, and a half cycle $\Phi_2$ is left for quantization and the following digital operation. In $\Phi_2$, since the two-stage class A/AB OTA is idle, it is cut off in this phase to save power. $C_S$, $C_{fb1i}$ and $C_{fb2i}$ are $2\,C_U$, $3\,C_U$ and $C_U$, respectively.

## 5 Simulation results

The proposed single-OTA no-DEM SDM was designed and simulated at transistor level under the design conditions shown in Table I. Using a −8 dBFS and 26.5625 kHz sinusoidal differential signal as input, the simulated output spectrum is displayed in Fig. 2 (c) which gives the peak SNDR. Here, $3^{rd}$-order noise shaping can be observed and harmonics caused by unit element mismatches in the feedback DACs are suppressed. Table I summarizes the performance of achieved SDM, while 100.2 dB dynamic range can be extracted from SNDR versus input amplitude diagram. A $3^{rd}$-order single-OTA SDM [6] with the similar parameters is listed in Table I for comparison, and the FOM is defined as Power/$(2^{(ENOB+1)} \bullet$ bandwidth), where ENOB = (SNDR − 1.76)/6.02 is the effective number of bits. Through comparison, the effectiveness of this work can be validated.

**Table I.** Modulator performance summary and comparison.

| Parameter | [6] | This work |
|---|---|---|
| Supply Voltage (V) | 3.3 | 1.2 |
| Technology | 0.35μm CMOS | smic 0.13μm CMOS |
| Sampling Frequency (Hz) | 3.25 M | 25.6M |
| Signal bandwidth (Hz) | 100k | 100k |
| Peak SNDR (dB) | 96 | 98.4 |
| Power consumption (mW) | 1 | 1.2 |
| Figure-of-Merit (fJ/conv-step) | 96.97 | 88.25 |

## 6 Conclusion

To shape feedback DAC mismatch of SDM, analog differentiators can be used in the branches of DAC at a cost of extra delay and complexity inducted by the in-loop digital compensatory integrator. Using an extra integrator in loop filter and a simple digital differentiator outside the loop of SDM, the above in-loop digital integrator can be avoided. A delay path capacitor mismatch insensitive triple integrator is proposed to lower power consumption caused by the extra analog integrator. Circuit level simulation based on 0.13 $\mu$m CMOS validated the effectiveness of this work.


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