

Dual-channel-output all-optical logic AND gate at 20 Gbit/s based on cascaded second-order nonlinearity in PPLN waveguide

J. Wang, J. Sun, Q. Sun, D. Wang, M. Zhou, X. Zhang, D. Huang and M.M. Fejer

Proposed and demonstrated is a novel scheme of a dual-channel-output all-optical logic AND gate. Using cascaded sum- and difference-frequency generation in a periodically poled lithium niobate (PPLN) waveguide, 20 Gbit/s logic AND operation with dual-channel outputs is successfully observed in the experiment.

Introduction: All-optical signal processing is a key technology in future high-speed optical communication networks. The all-optical logic AND gate is one of the crucial elements for all-optical signal processing. Recently, various approaches have been explored to enable logic AND operation, including use of semiconductor optical amplifiers (SOAs) [1, 2], semiconductor microresonators [3], and periodically poled lithium niobate (PPLN) waveguides [4–8]. These schemes have shown impressive operation performance. However, only single-channel AND output can be obtained. It is well known that PPLN-based all-optical signal processing has several distinct advantages of ultrafast response, no excess noise, and great flexibility owing to various second-order nonlinearities and their cascading. In this Letter, we report a novel dual-channel-output logic AND gate by using cascaded sum- and difference-frequency generation (SFG + DFG) in a PPLN waveguide. 20 Gbit/s logic AND operation with dual-channel outputs is demonstrated in the experiment.

Experimental setup and operation principle: The proposed SFG + DFG-based logic AND gate is illustrated in Fig. 1. Two pseudorandom binary sequence (PRBS) return-to-zero (RZ) signals (X , Y) at 20 Gbit/s are generated from two tunable lasers (TLs) modulated by two cascaded Mach-Zehnder modulators (MZMs). The data and clock signals used to drive the MZMs are provided by a bit pattern generator (BPG). After being amplified by an erbium-doped fibre amplifier (EDFA), two PRBS RZ signals are divided into two paths by a wavelength division multiplexer (WDM) with one path delayed integral bit periods with respect to the other by an optical delay line (ODL). An external cavity laser (ECL) is used to generate a continuous-wave (CW) control light. All three input optical waves, i.e. signal X , signal Y and CW control, are combined by an optical coupler (OC) and then launched into the PPLN waveguide to participate in the SFG + DFG processes after passing through a high-power EDFA (HP-EDFA) and a polarisation controller (PC). The commercial HP-EDFA can provide a small-signal gain of 40 dB and a saturation output power of 30 dBm. The PC inserted before the PPLN is used to adjust the polarisation states of optical waves in order to enhance the nonlinear interactions inside the PPLN waveguide. A 50 mm-long PPLN waveguide fabricated by the electric-field poling method and annealing proton-exchanged (APE) technique is adopted in the experiment. It has a microdomain period of 14.7 μm , a waveguide width of 12 μm , an initial proton exchange depth of 0.8 μm , and a quasi-phase matching (QPM) wavelength of 1543.2 nm at room temperature. The fibre-to-fibre coupling loss is estimated at about 4.7 dB, caused by reflection losses at the uncoated end faces, mode mismatching between the fibres and the PPLN waveguide, and intrinsic waveguide losses. The optical spectra are monitored by an optical spectrum analyser (OSA), (Anritsu MS9710C) with the highest spectral resolution of 0.05 nm. The temporal waveforms are observed by a communications signal analyser (CSA), (Tektronix 8000B). Two variable optical attenuators (VOAs) are used to control the optical powers entering into the OSA and CSA.

The operation principle of the proposed dual-channel-output logic AND gate can be briefly described as follows. As shown in Fig. 1, two input signals (λ_{SX} , λ_{SY}) are set close to each other, because of which the SFG process between the CW control (λ_C) and signal Y is almost quasi-phase matched when the CW control and signal X satisfy the SFG QPM condition. As a result, there exist two kinds of SFG + DFG processes. Both signal X and signal Y interact with the CW control through SFG to generate two sum-frequency waves (SF1 and SF2). Meanwhile, signal Y

and SF1 as well as signal X and SF2 take part in the subsequent DFG process to produce two idler waves (idler 1 and idler 2) with their wavelengths determined by $1/\lambda_{i1} = 1/\lambda_{SX} + 1/\lambda_C - 1/\lambda_{SY}$ and $1/\lambda_{i2} = 1/\lambda_{SY} + 1/\lambda_C - 1/\lambda_{SX}$, respectively. The dual-channel idler waves can be filtered by use of a tunable filter (TF) with a 3 dB line width of 0.3 nm. Note that for each of the two SFG + DFG processes, the new idler wave is achieved only when all three optical waves (signal X , signal Y , and CW control) are present. Thus the obtained dual-channel idler waves can actually be regarded as the logic AND results of signal X and signal Y , which indicates implementation of the dual-channel-output logic AND gate.

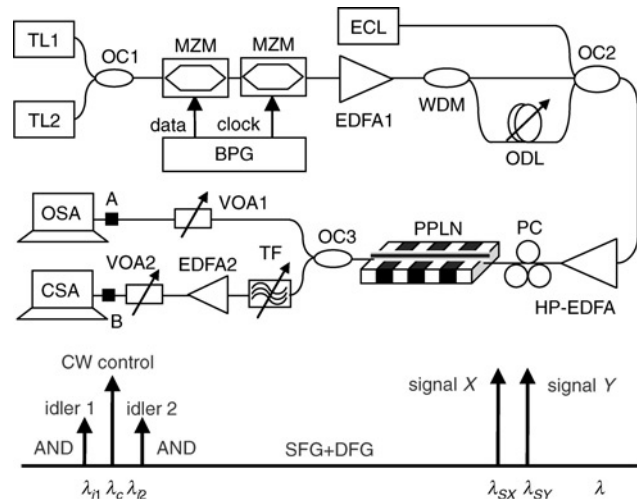


Fig. 1 Experimental setup for SFG + DFG-based dual-channel-output logic AND gate

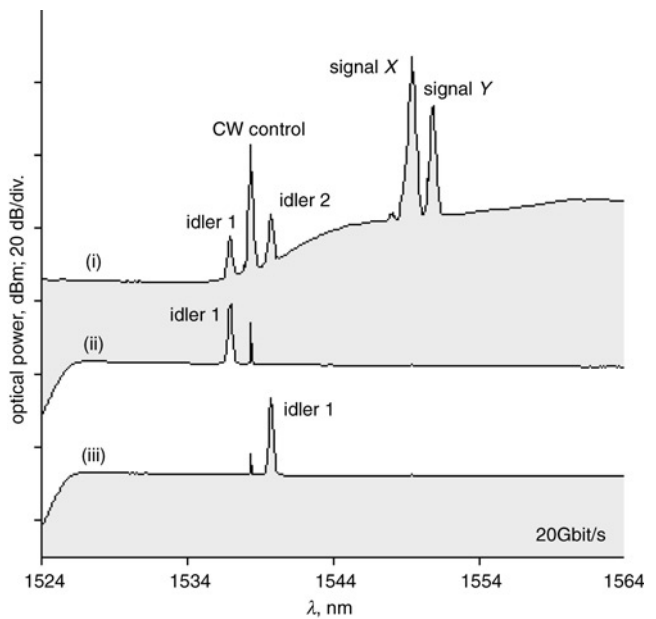


Fig. 2 Measured optical spectra for SFG + DFG-based dual-channel-output logic AND gate (wavelengths of signal X , signal Y , and CW control are 1549.4, 1550.9, 1538.3 nm, respectively; two idler waves generated at 1537.0 and 1540.0 nm, respectively)

- (i) Output optical spectrum from PPLN measured at point A in Fig. 1
- (ii) Optical spectrum of idler 1 measured at point B in Fig. 1
- (iii) Optical spectrum of idler 2 measured at point B in Fig. 1

Experimental results: Fig. 2 shows the typical measured optical spectra for the SFG + DFG-based dual-channel-output logic AND gate. As shown in Fig. 2, (i), which is measured at point A in Fig. 1, the CW control and signal X are set at 1538.3 and 1549.4 nm, respectively, to meet the SFG QPM condition. Signal Y is tuned at 1550.9 nm, which is close to signal X . It is found that dual-channel idler waves are generated at 1537.0 and 1540.0 nm, respectively, thanks to the two kinds of SFG + DFG nonlinear interactions. Fig. 2, (ii) and (iii), which are measured at point B in Fig. 1, depict

the spectra for filtered dual-channel-output idler waves. Fig. 3 further presents the measured temporal waveforms for input signal *X*, signal *Y*, and dual-channel idler waves. According to the current lab conditions, 20 Gbit/s 2^7-1 PRBS RZ signals are employed. The scale in Fig. 3 is 200.0 ps/div. It can be clearly seen from Fig. 3 that a dual-channel-output logic AND gate is successfully demonstrated in the experiment.

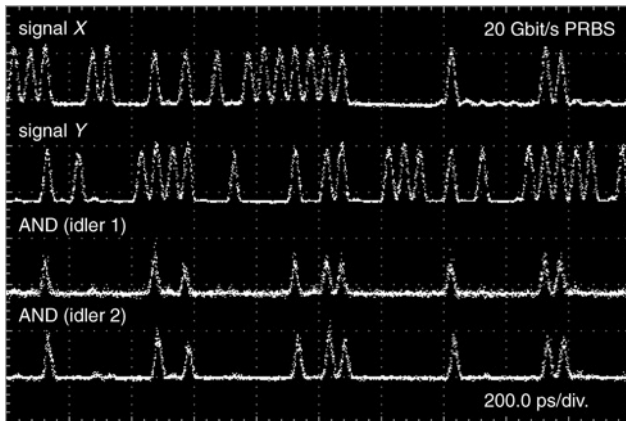


Fig. 3 Measured temporal waveforms for input signal *X*, signal *Y*, and dual-channel output idlers with logic AND results

With further improvement, the dual-channel-output logic AND gate can also potentially be implemented by properly adjusting signal *Y* to be close to CW control. In addition, it is also possible to perform the logic AND operation at 40 Gbit/s or much higher speed owing to the ultrafast response characteristic of the PPLN waveguide.

Conclusion: By using SFG + DFG in a PPLN waveguide and setting two signals close to each other, we propose and have demonstrated a novel dual-channel-output logic AND gate. Both optical spectra and temporal waveforms observed in the experiment imply successful implementation of logic AND operation at 20 Gbit/s with dual-channel outputs. The obtained results may stimulate future wide researches on PPLN-based all-optical logic gates.

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