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Dual track architecture and time synchronous scheme for wavelet reconstruction processor using SAW device based on MSC

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ABSTRACT

In this paper, we propose dual track architecture and time synchronous scheme for wavelet reconstruction processor using surface acoustic wave (SAW) device based on multistripe coupler (MSC). An arbitrary scale wavelet reconstruction processor with dual track architecture consists of a wavelet interdigital transducer (IDT) apodized by the envelope of wavelet function, two MSCs, and two reconstruction wavelet IDTs apodized by the envelope of identical reconstruction wavelet function. The SAW launched by wavelet IDT is bidirectional. Two reconstruction wavelet IDTs with identical design parameter are symmetrically deposited on the dual track of wavelet reconstruction processor. Therefore, the performances of wavelet reconstruction processor were improved due to bidirectional SAW received by two reconstruction wavelet IDTs. Furthermore, the delay time characteristic of SAW propagating on crystals substrate surface was skillfully applied to compensate the time asynchronous problem among wavelet reconstruction processor. This means ensures that all scale processors in wavelet reconstruction processor have identical response time. An experiment of wavelet reconstruction processor with dual track architecture and time synchronous scheme was presented. Experimental results confirm that the performances of wavelet reconstruction processor are improved, and time synchronous is realized in this wavelet reconstruction processor with three scales.

1. Introduction

Wavelet technology can process and character non-stationary signals in both the time and frequency domain, and can analyzes low frequencies signals in wide time windows and high frequencies ones in narrow time windows, thus it has received considerable attention and application in science research and engineering application fields [1–3]. In most cases, it is necessary that signal can be recovered from the wavelet transform result at a scale or multiscale, such as signal and image processing [2], data compression [4] and noise removal [5,6]. However, the wavelet reconstruction algorithm to need a larger number of mathematic operation and complicated program was normally realized by computers and related software. Thus it is very complicated and difficult for technologists and actual engineering applications.

In order to solve these problems, some schemes have been developed to implement wavelet reconstruction with various physical devices such as very large scale integration (VLSI) [7,8], and optical lens [9,10]. Although the wavelet reconstruction realized by VLSI and optical lens is good choice for the signal processing devices, there are some problems, such as the power and memory limitation of VLSI, and the device size and frequency limitation due to the cutoff frequency of optical lens.

In our previous works [11], a scheme of implementing wavelet reconstruction with surface acoustic wave (SAW) device based on multistripe couplers (MSC) has been proposed. However, as the carrier of wavelet reconstruction processor, the SAW device also suffers some problems such as second-order effects, bulk wave effects and high loss. These problems can produce spurious acoustic signals and some ripples in response curve, and can destroy the performances of wavelet reconstruction processor. In order to improve the processor performances, dual track architecture of wavelet reconstruction processor using SAW device based on MSC is proposed and realized in this paper.

For an arbitrary scale processor, the response time should be equal to the transit time of the SAW propagating on the sur-

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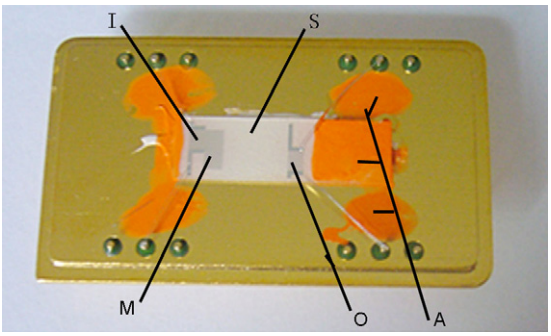

Fig. 1. Interior architecture of wavelet reconstruction processor using SAW device based on MSC at scale $s = 2^{-8}$. I is wavelet IDT. M is full transfer MSC, and O is reconstruction wavelet IDT, and S is the 128°Y-X $LiNbO_3$ crystals substrates, and A is the absorption material.

face of crystals substrate. However, the geometrical architecture is different to different scale processors in wavelet reconstruction processor, thus the trigger time that equals the transit time of SAW excited by same signal is not equal to different scale processors. In this case, the wavelet reconstruction results cannot recover signal correctly due to not having identical time parameters, i.e., wavelet reconstruction processor is time asynchronous. Hence, we further studied the time asynchronous problem, and presented a synchronous compensation scheme for wavelet reconstruction processor using SAW device based on MSC according to the delay time characteristic of SAW propagating on crystals substrate surface.

2. Principles of wavelet reconstruction processor using saw device based on MSC

According to SAW theory, the frequency response of interdigital transducer (IDT) equals the Fourier transform of the envelope function of IDT, and the frequency response of SAW device with MSC is the product of the transfer functions of two apodized IDTs [12–15]. In Ref. [11], we proposed to implement wavelet reconstruction with SAW device based on MSC. Fig. 1 shows the interior architecture of wavelet reconstruction processor using SAW device based on MSC at scale $s = 2^{-8}$.

Fig. 2 is the frequency response curve for the wavelet reconstruction processor in Fig. 1, which is obtained by network analyzer (Advantest R3765CG). In the frequency response curve, we can see some ripples that arise from second-order effects, the triple transit

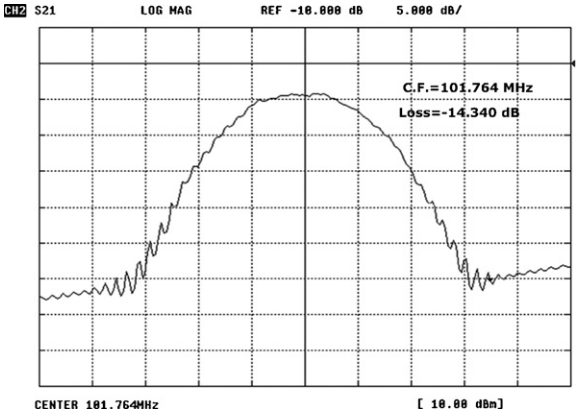

Fig. 2. Frequency response curve for wavelet reconstruction processor at scale $s = 2^{-8}$.

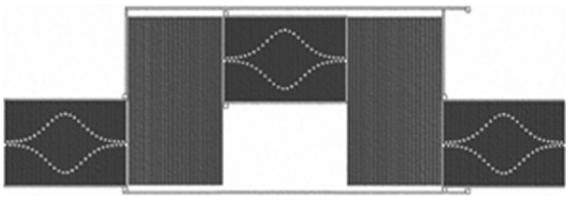

Fig. 3. Layout of a scale wavelet reconstruction processor using SAW device based on MSC with dual track architecture.

signals, etc. In addition, the processor has high insertion loss (IL) due to only receive part of bidirectional SAW launched.

3. Dual track architecture of wavelet reconstruction processor using SAW device based on MSC

As the carrier of wavelet reconstruction processor, SAW device play an important role in the performances of wavelet reconstruction processor. For example, the second-order effects and bulk wave effects can produce spurious acoustic signals and some ripples in response curve, and can destroy the performances of wavelet reconstruction processor. Some methods were already used in wavelet reconstruction processor using SAW device based on MSC: the phase front distortion eliminated by dummy electrodes, and acoustic reflections minimized by split electrodes, etc., but the triple transit signals still could not be eliminated. Furthermore, the unidirection receiving will result in 6 dB insertion loss. In order to solve problems above and improve processor performance, we developed a dual track architecture for wavelet reconstruction processor using SAW device based on MSC, as shown in Fig. 3. The layout was designed with L-edit. The wavelet reconstruction processor using SAW device based on MSC consists of a wavelet IDT apodized by the envelope of wavelet function, two MSCs, and two wavelet reconstruction IDTs with same design parameters. Two wavelet reconstruction IDTs were apodized by the envelope of identical reconstruction wavelet function.

Since the MSC may fully transfer SAW without affecting BAW continuing to propagate in the primitive acoustic track, the SAW and BAW launched by wavelet IDT can be separated into different tracks. Therefore, one can spread some sound absorption material at the transmission terminal of BAW, and can ultimately eliminate the BAW that interferes with the response performance of wavelet reconstruction processor.

Another main problem of wavelet reconstruction processor is the presence of triple transit signal arising from multiple acoustic reflections between wavelet and wavelet reconstruction IDTs. It is possible to suppress triple transit signal using the dual track architecture in Fig. 3.

When signal is fed into wavelet IDT, the full transfer MSC M_1 and M_2 will transfer the SAW into wavelet reconstruction IDT O_1 and O_2, respectively. The acoustic wave signal L_1 and L_2 will simultaneously be reflected by two output IDTs, as shown in Fig. 4, and can be

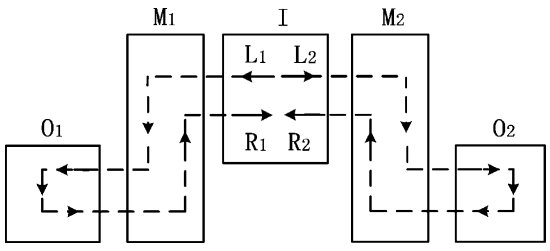

Fig. 4. Principles of suppressing triple transit signal.

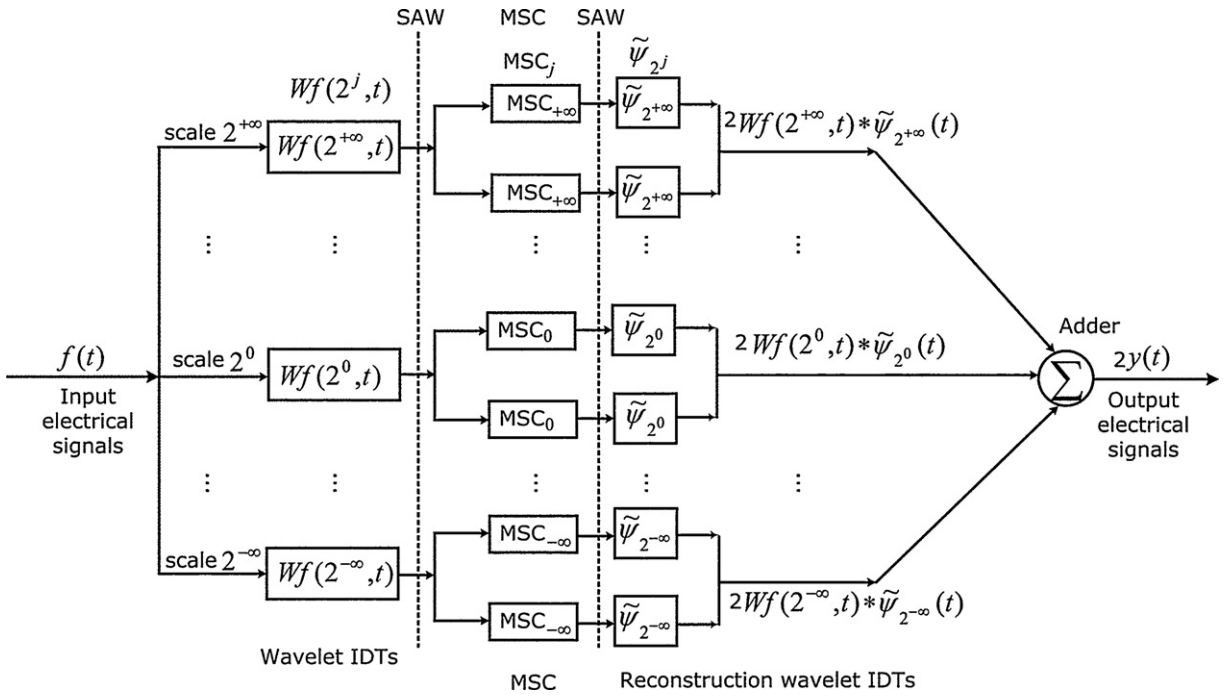

Fig. 5. Schematic diagram of multiscale wavelet reconstruction processor using SAW device based on MSC with dual track architecture.

coupled to the input IDT via MSC again. Because the bidirectional acoustic signal were launched by input IDT at the same time, and the MSC and output IDT have identical structure and parameters, the two reflection acoustic waves equal in energy and opposite in direction, i.e.,

$$R_1 = -R_2. \tag{1}$$

Fig. 4 and Eq. (1) indicate that triple transit signal generated by two wavelet reconstruction IDTs must be offset in input IDT. Thus we call input IDT is now a perfect absorber of the acoustic signals reflected from the O_1 and O_2.

Since the output electrodes of O_1 and O_2 are in parallel connection in Fig. 3, the bidirectional SAW launched by wavelet IDT would be totally received. The insertion loss will reduce 3 dB to a single output IDT in Fig. 1 without considering the location effect and the phase difference between two output tracks.

The structure of dual track was used in this scheme, thus, the receiving energy will be twice as much as that of wavelet reconstruction processor in Fig. 1. Fig. 5 shows the schematic architecture of multiscale wavelet reconstruction processor using SAW device based on MSC with dual track architecture.

4. Time asynchronous problem and compensation scheme for wavelet reconstruction processor

4.1. Time asynchronous problem in wavelet reconstruction processor

The structure of dual track is identical in Fig. 3, thus we here only analyze one track of the wavelet reconstruction processor using SAW device based on MSC. When an input signal $f(t)$ is applied to the processor, as shown in Fig. 6, wavelet transform operation would be implemented at the wavelet IDT firstly. By means of the inverse piezoelectric effects, the wavelet transform result $Wf(2^j,t)$ will be converted into SAW propagating on the piezoelectric crystals. The SAW signal $Wf(2^j,t)$ will be coupled into the output IDT via full transfer MSC and the transform result will be reconstructed in wavelet reconstruction IDT. Simultaneously, the signal was reconverted into electrical signal $X(2^j,t)$, which readily be received and processed subsequently. Hence, the trigger time of processor should be equal to the transit time of SAW propagating on the piezoelectric substrate.

In Fig. 6, the transit time of SAW propagating on the piezoelectric substrate is

$$t_j = \frac{L_{ij}}{2V} + \frac{L_{imj}}{V_s} + \frac{L_{mj}}{V} + \frac{L_{moj}}{V_s} + \frac{L_{oj}}{2V}, \tag{2}$$

where V_s is the velocity of SAW propagating on free crystals surface, V is the velocity of SAW propagating on alternate metal electrodes and free surface. When the ratio of the metal electrode width to the transducer half period is 0.5, V could be obtained from

$$V = \frac{2V_s V_m}{V_s + V_m}. \tag{3}$$

The SAW velocity V_m for SAW propagating on metallic surface is given by

$$V_m = V_s\left(\frac{2-K^2}{2}\right), \tag{4}$$

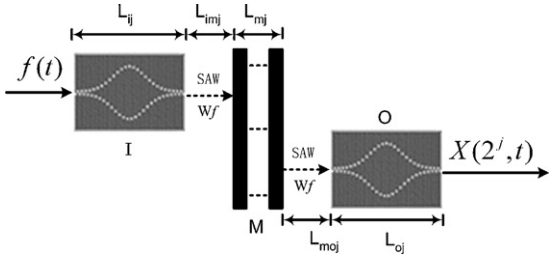

Fig. 6. SAW propagating on the one track of wavelet reconstruction processor using SAW device based on MSC. 'I' is wavelet IDT, and 'L_{ij}' is its length. 'M' is MSC, and 'L_{mj}' is its width. 'O' is reconstruction wavelet IDT, and 'L_{oj}' is its length. 'L_{imj}' is the distance between wavelet IDT and MSC. 'L_{moj}' is the distance between MSC and reconstruction wavelet IDT.

where K^2 is the electromechanical coupling constant of the substrate material.

According to Eqs. (3) and (4), velocity value V_s and V only depend on the substrate material. Thus the total transit time value t_j will be determined by these parameters: L_{ij}, L_{imj}, L_{mj}, L_{moj} and L_{oj}.

In the implementation of an arbitrary scale wavelet reconstruction processor, although the envelope magnitude of reconstruction wavelet IDT is 2/(A+B) that of wavelet IDT, the envelope length of reconstruction wavelet IDT is equal to that of wavelet IDT. In addition to early wavelet reconstruction processor, the gap distance between wavelet IDT and MSC, and the gap distance between MSC and reconstruction wavelet IDT are equal to a wavelength value of SAW at acoustic synchronous frequency, thus we have

$$L_{ij} = L_{oj}, \tag{5}$$

$$L_{imj} = L_{moj} = \lambda_{0j}, \tag{6}$$

where λ_{0j} is a wave length value of SAW propagating on the free piezoelectric substrate, $\lambda_{0j=}V_s/f_j$, f_j is the centre frequency of wavelet reconstruction processor at scale 2^j.

In order to study the time asynchronous problem, as an example, the transit time difference between scale 2^0 and 2^j processors is derived.

From Eqs. (2), (5) and (6), the transit time of SAW propagating on the scale 2^0 and 2^j processors, respectively, are given by

$$t_0 = \frac{L_{i0}}{V} + \frac{2\lambda_{00}}{V_s} + \frac{L_{m0}}{V}, \tag{7}$$

$$t_j = \frac{L_{ij}}{V} + \frac{2\lambda_{0j}}{V_s} + \frac{L_{mj}}{V}. \tag{8}$$

Although the length of wavelet IDT depends on that of the envelope of wavelet function, on the basis of scale dyadic dilation, the lengths of two arbitrary scale wavelet IDTs are related closely each other. For example, the envelope of Morlet wavelet function is

$$A_{2^j}(t) = \frac{1}{2^j}\ \exp\left(-\frac{1}{2}\left(\frac{t}{2^j}\right)^2\right). \tag{9}$$

Eq. (9) indicates the envelope length will doubly increase or doubly reduce with scale dyadic dilation. Hence, the relationship between L_{i0} and L_{ij} are as follows:

$$L_{ij} = 2^j L_{i0}. \tag{10}$$

According to Refs. [15] and [16], we have

$$L_{mj} = \frac{2\lambda_j}{K^2}, \tag{11}$$

where λ_j is a wave length value of SAW propagating on the MSC, λ_j=V/f_j.

$$f_j = 2^{-j} f_0. \tag{12}$$

According to the above analysis, the transit time that SAW propagating on scale 2^j processor is not equal to that of scale 2^0 processor. The transit time difference between scale 2^j and scale 2^0 processor can be given by

$$\Delta t_{0,j} = \left|t_0 - t_j\right| = \frac{\left|(1-2^j)\right|\left(f_0 K^2 L_{i0} + 2VK^2 + 2V\right)}{f_0 K^2 V} \tag{13}$$

Since all parameters in Eq. (13) are not zero, the transit time difference $\Delta t_{0,j}$ is not zero, i.e., the wavelet reconstruction processor using SAW device based on MSC is time asynchronous.

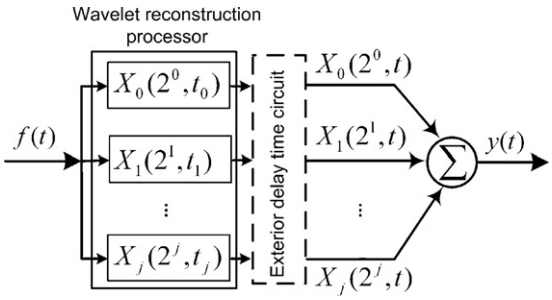

Fig. 7. Schematic diagram of delay time compensation using exterior delay time circuits.

4.2. Delay time compensation scheme for wavelet reconstruction processor

For an arbitrary scale wavelet reconstruction processor, the response time should be equals to the transit time of SAW propagating in this scale processor. However, the transit time is different to different scale processor due to not having same geometrical architecture. When input signal $f(t)$ is applied to the wavelet reconstruction processor, the time asynchronous problem was presented. Hence, the actual wavelet reconstruction results outputted by every scale processor are $X(2^0,t_0)$,. . ., $X(2^j,t_j)$ $(t_0 \neq \ldots \neq t_j)$, without being $X(2^0,t)$,. . ., $X(2^j,t)$. Although the time asynchronous problem of wavelet reconstruction processor could be generally solved by exterior delay time circuit part, as shown in Fig. 7, the scheme increases the size, power consuming and weight. On the other hand, twice compensation with exterior delay time circuit complicates implementing procedure. Hence implementing time synchronization with exterior delay time circuit is not optimization scheme.

An extraordinary property of a SAW is its extremely low velocity about 10^5 times smaller than those of electromagnetic waves [12,15]; therefore, SAW possess extremely small wavelengths compared with electromagnetic waves at the same frequency. The advantage characteristics make SAW device dramatic reductions in size and weight when compared with electromagnetic device. In addition, the electrical signal and SAW signal could readily be converted by IDT each other, so we can control the delay time by adjusting the distance between MSC and reconstruction wavelet IDT. Based on these advantages above, SAW device is wildly applied to communication system, radar, portable electronic equipment, sensors, etc. [15,17].

Hence, the transit time difference $\Delta t_{0,j}$ between scale 2^j processor and scale 2^0 processor in Eq. (13) could be compensated by delay time characteristic of SAW propagating on crystal substrate surface.

If we know the design parameters of wavelet reconstruction processor for scale 2^0, according to Eqs. (7), (8), (11)–(13), the compensation distance between MSC and reconstruction wavelet IDT for scale 2^j processor is

$$\Delta L_{moj} = \begin{cases} +\left|V_s \Delta t_{0,j}\right|, & j < 0 \\ 0, & j = 0 \\ -\left|V_s \Delta t_{0,j}\right|, & j > 0 \end{cases}. \tag{14}$$

In order to keep time synchronization between scale 2^j processor and scale 2^0 processor, the design distance value between MSC and reconstruction wavelet IDT for scale 2^j processor should be

$$L_{moj} = \begin{cases} L_{mo0} + \left|V_s \Delta t_{0,j}\right|, & j < 0 \\ L_{mo0}, & j = 0 \\ L_{mo0} - \left|V_s \Delta t_{0,j}\right|, & j > 0 \end{cases}. \tag{15}$$

Using a similar method, the parameter expression of compensation time asynchronous problem between two arbitrary scale processors in wavelet reconstruction processor could be derived and presented. If all design parameters is provided for scale 2^j in the wavelet reconstruction processor consisting of $|n|+1 (n \in Z)$ scale, from Eqs. (10)–(12), the transit time difference between SAW propagating on scale 2^{j+n} processor and that on another scale 2^j processor is

$$\Delta t_{j,(j+n)} = \left| t_j - t_{(j+n)} \right| = \frac{\left|(1-2^n)\right| (f_j K^2 L_{ij} + 2VK^2 + 2V)}{f_j K^2 V}. \quad (16)$$

In order to keep time synchronization between scale 2^j processor and scale 2^{j+n} processor, the compensation distance between MSC and reconstruction wavelet IDT for scale 2^{j+n} processor should be

$$\Delta L_{mo(j+n)} = \begin{cases} +\left|V_s \Delta t_{j,(j+n)}\right|, & n < 0 \\ 0, & n = 0 \\ -\left|V_s \Delta t_{j,(j+n)}\right|, & n > 0 \end{cases}. \quad (17)$$

Hence, the design distance between MSC and reconstruction wavelet IDT for scale 2^{j+n} processor is

$$L_{mo(j+n)} = \begin{cases} L_{moj} + \left|V_s \Delta t_{j,(j+n)}\right|, & n < 0 \\ L_{moj}, & n = 0 \\ L_{moj} - \left|V_s \Delta t_{j,(j+n)}\right|, & n > 0 \end{cases}. \quad (18)$$

According to Eqs. (17) and (18), we can readily implement a time synchronous wavelet reconstruction processor using SAW device based on MSC with dual track architecture.

5. Experiments

In order to confirm the dual track architecture and time synchronous scheme for wavelet reconstruction processor using SAW device based on MSC, we here present a wavelet reconstruction processor consisting three scale processors: scale 2^{-7}, 2^{-8}, and 2^{-9} processor.

The three scale processors were fabricated on 128°Y-X $LiNbO_3$ crystal substrates, respectively. The velocity V_s of SAW propagating on 128°Y-X $LiNbO_3$ substrate is 3980 m/s, and electromechanical coupling constant K^2 is 5.5%. The configuration parameters for scale 2^{-7}, 2^{-8} and 2^{-9} processor are shown in Table 1. The transit time of SAW propagating on the scale 2^{-7} processor is regarded as the trigger time of wavelet reconstruction processor. Where $\Delta L_{mo(j+n)}$ is the compensation distance; L_{moj1} and L_{moj2} denotes the distance L_{moj} for uncompensated and compensated scale devices, respectively. A, B, C denotes scale 2^{-7}, 2^{-8} and 2^{-9} wavelet reconstruction processor, respectively. Dummy electrodes were used as eliminate the phase front distortion of waves propagating through apodized IDTs, and split electrodes were used as minimize acoustic reflections within transducers. Aluminum IDTs, with uniform spacing and metallization ration of 50%, were directly deposited by projection electron beam photolithography on the top of 128°Y-X $LiNbO_3$ substrate.

Table 2 shows the transit time of SAW propagating on the uncompensated and compensated wavelet reconstruction processor. Where $\Delta t_{j,(j+n)}$ is the transit time difference between scale 2^{-7} and other scale processors; t_{moj1} and t_{moj2} denotes the transit time t_{moj} for SAW propagating on uncompensated and compensated scale processors, respectively.

Table 1
Configuration parameters for uncompensated and compensated scale processors

	Scale processors		
	A	B	C
f_j (MHz)	50.88	101.76	203.52
L_{ij} (mm)	2.42	1.21	0.60
Electrodes width (μm)	9.776	4.888	2.444
Number of electrodes pairs	256	256	256
L_{imj} (μm)	76.38	38.19	19.09
L_{mj} (mm)	3.00	1.50	0.75
Width of MSC electrodes (μm)	14.32	7.16	3.58
Number of MSC electrodes	103	103	103
L_{moj1} (μm)	76.38	38.19	19.09
$\Delta L_{mo(j+n)}$ (mm)	0.0	2.865	4.297
L_{moj2} (mm)	0.076	2.903	4.316
L_{oj} (mm)	2.42	1.21	0.60

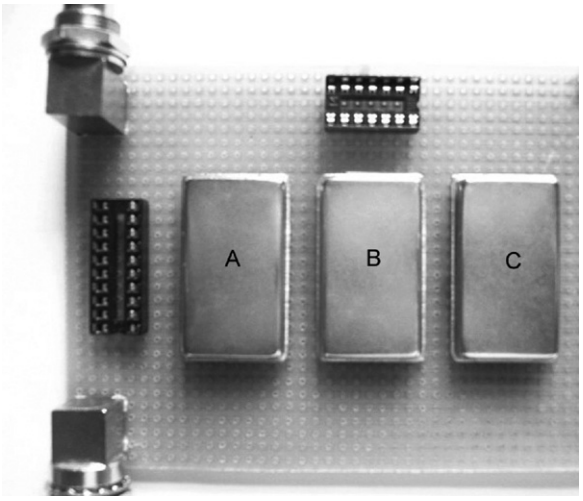

Fig. 8. Time synchronous wavelet reconstruction processor using SAW device based on MSC with dual track architecture and time synchronous scheme.

Fig. 8 shows the wavelet reconstruction processor using SAW device based on MSC with dual track architecture and time synchronous scheme. In order to compare with the frequency response curve in Fig. 2, the frequency response curve for wavelet reconstruction processor at scale $s = 2^{-8}$ is measured by the network analyzer (Advantest R3765CG), as shown in Fig. 9.

Since the triple transit signal is suppressed, for wavelet reconstruction processor using SAW device based on MSC with dual track architecture and time synchronous scheme, we can observe that the passband ripples and sidelobes in frequency response curve is smaller than ones of single track processor in Fig. 2. In addition, the bidirectional SAW launched by wavelet IDT would be totally received, thus the insertion loss is decreased from 14.340 dB to 12.126 dB.

Appling trigger signal to the wavelet reconstruction processor, we can examine trigger time for three scale processors at rising edge time by oscilloscope (Agilent-MSO6104A), as shown in Fig. 10.

Table 2
Transit time of SAW propagating on uncompensated and compensated scale processors

Scale processors	t_{ij} (μs)	t_{imj} (μs)	t_{mj} (μs)	t_{moj1} (μs)	$\Delta_{j,(j+n)}$ (μs)	t_{moj2} (μs)	t_{oj} (μs)
A	0.3177	0.0197	0.7861	0.0197	0.0	0.3177	0.3177
B	0.1589	0.0098	0.3931	0.7501	0.7304	0.1589	0.1589
C	0.0794	0.0049	0.1965	1.1153	1.0957	0.0794	0.0794

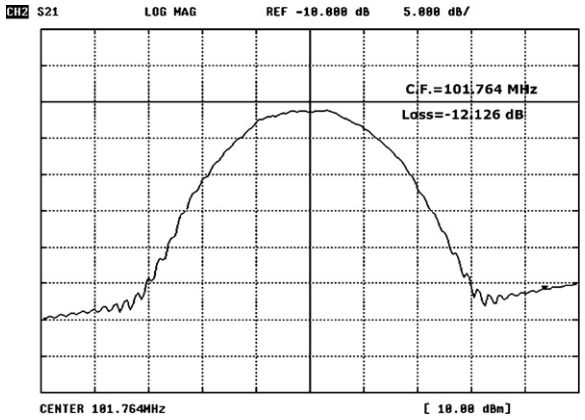

Fig. 9. Frequency response curve of wavelet reconstruction processor using SAW device based on MSC with dual track architecture and time synchronous scheme at scale $s = 2^{-8}$.

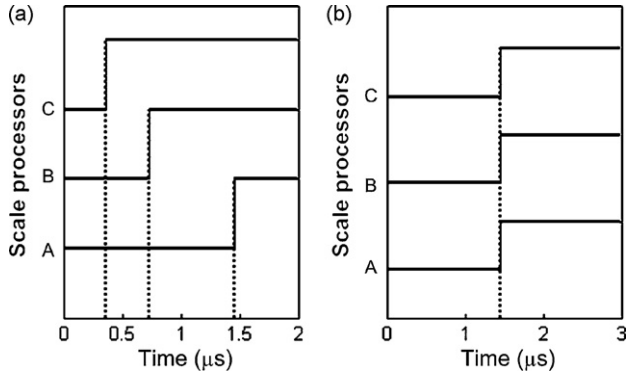

Fig. 10. Trigger time detection at the rising edge time. (a) Trigger time for uncompensated processors and (b) trigger time for compensated processors.

Fig. 10(a) illustrates that uncompensated wavelet reconstruction processor is time asynchronous, in particular, the maximal response time difference between 2^{-7} processor and 2^{-9} processor is about 1.1 μs. Fig. 10(b) shows that all scale processors in compensated wavelet reconstruction processor using SAW device based on MSC have identical trigger time, i.e., compensated wavelet reconstruction processor using SAW device based on MSC is time synchronous.

6. Conclusions

In this paper, we have presented the dual track architecture and time synchronous scheme for wavelet reconstruction processor using SAW device based on MSC. The basic principle of our technology is that the SAW signals excited by input IDT will be bidirectional, and bulk wave effects can be suppressed by MSC. Moreover, the delay time characteristic of SAW propagating on crystal substrate surface was skillfully applied to compensate the time asynchronous problem among wavelet reconstruction processor, which ensures that all scale processors have identical response time. These schemes avoid a large number of mathematic operation and complicated program in wavelet technology applications. Wavelet reconstruction processor using SAW device based on MSC benefits from the excellent properties of SAW devices: passive, small size, real-time, high reproducibility and high reliability, which overcomes the memory limitation, high cost and high power for VLSI, and avoids the big size and frequency limitation of optical lens. Furthermore, the SAW fabrication technology based on photolithographic and microelectronic makes it be very interesting objects for further investigations.

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