A New Design of Voltage Controlled Oscillator

WU xiulong, CHEN Junning, MEI Zhenfei, ZHAO Yuhao, XU Tailong
Institute of Electronic Science and Technology
Anhui University
Hefei, China
e-mail : xiulong@ahu.edu.cn

Abstract—**This paper designed a new low phase noise voltage-controlled oscillator (VCO) with harmonic filtering resistor and source damping resistor. The author analyzed and modulated the results by the simulator of Mentor Graphics in a 0.35-um CMOS process, and achieved the optimization scheme in the end. The simulation result shows the VCO can reach a phase noise of -124.9dBc/Hz at 1MHz offset while working at 4.6GHz in a 3mA excursion current. During the 0 to 3 controlled voltage the tuning range can reach 18.5%, and the power consumption is only 7.09mW.**

Keywords- phase noise; harmonic filtering resistor; damping resistor

I. INTRODUCTION

In modern communication systems, VCOs are the essential building blocks for frequency translation. Even though the performance of RF CMOS transistor has been improved, the inherent $1/f$ noise is still an obstacle to the design of an integrated high performance VCO. As CMOS downscaling is in progress for high level integration at low cost, the corner frequency of the small-size transistors tends to increase and this becoming one of the most important factor to restrict the improvement of VCOs.

Recently, many methods were used to decrease the influence of the phase noise. Such as the capacitive coupling to suppress the $1/f$ noise up-conversion in the differential LC oscillator [1], the on chip high Q conductance[2] and so on.

This work proposed a low phase noise and low power dissipation VCO composed of high performance harmonic filtering resistor and source damping resistors.

II. THE PHYSICAL PROCESS OF THE PHASE NOISE

As we known that the phase noise of the VCO is mainly introduced from various mixing phenomenon of the negative gm switching differential pair.

One of the most important mixing phenomenon is the up and down conversion of the thermal noise near the oscillator's frequency, and the other one is the up-conversion from flicking noise in the base band to the phase noise of the base frequency.

First let's think about the well known phase noise model for an oscillator as follows[3]:

$$L(\Delta\omega) \propto \frac{kTRF}{V_0^2} \cdot \left(\frac{\omega_0}{Q}\right)^2 \cdot \frac{1}{\omega_m^2} \qquad (1)$$

Where ω_m is the biasing frequency the phase noise was measured, ω_0 is the frequency of the VCO and T is the absolutely temperature.

However, this proportionality did not provide the exact solution to lower the phase noise, and thus, we defined the noise factor F as follows:

$$F = 2 + \frac{8\gamma IR}{\pi V_0} + \gamma\frac{8}{9} \cdot g_{mbias} \cdot R \qquad (2)$$

Where g_{mbias} is the trans-conductance of the biasing current source, the three parts of is generated by the resonator, differential pair and tail bias current respectively. This is also the dominating phase noise source in the oscillator. From the formula above we known that we can change the noise factor by change the g_{mbias}.

III. THE PROPOSED VCO AND OPTIMIZATION

The proposed VCO composed of all PMOS transistor because the PMOS transistor has lower phase noise than the NMOS transistor. The PMOS transistor has much restrain to the phase noise of the substrate because the current source of the PMOS biasing has been placed in the n well but not in the substrate. Furthermore, the PMOS transistor has much less flicking noise up-converted to the phase noise.

The biasing current source in the VCO has two functions. Firstly, it provides biasing circuit for the resonant. Secondly, it introduces high impedance for the switching pair transistor of the resonant in order to guarantee the output wave holding symmetry. But the tail current source can also bring much flicking noise. If the symmetry of the circuit is not good enough, the flicking noise will mixing with the oscillator's basic frequency and lead to the base band frequency noise near the oscillator's frequency.

Generally, we often use the LC filtering technology to reduce the noise effect of the tail current source which as shown in figure 1 [4].

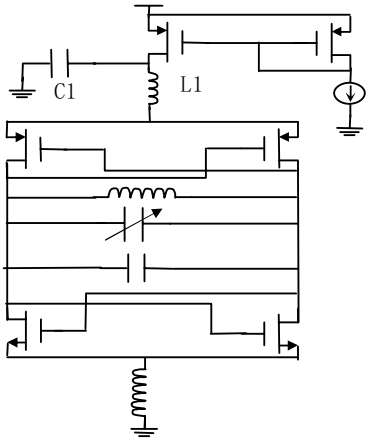

Figure1 The conventional structure of VCO

The C and L_1 in figure 1 can resonant at the frequency of $2\omega_0$ and provide a high impedance for the second harmonic to protect the quality factor of the LC resonant. The capacitance C inject in the common mode node of the biasing current source was used to restrain the up-convert of the high frequency harmonic produced by the current source noise. For the C can provide a low DC pass to the ground for the high harmonic.

However, the performance of the VCO shown in figure 1 was easily been restricted by the size of the chip, and the integrated single-ended inductor usually has a poor quality factor.

The proposed VCO adopted a harmonic filtering resistor R_1 to replace the filtering capacitance or inductance, and introduced source damping resistors such as R_2, R_3, R_4, R_5 as shown in figure 2.

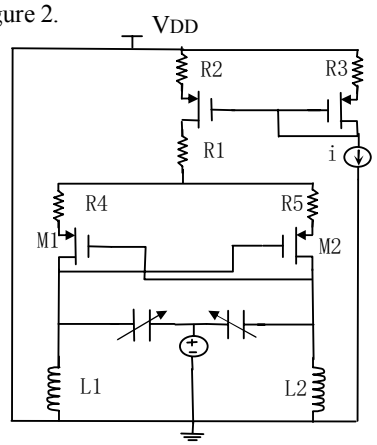

Figure 2 The proposed structure of VCO

As we known, the flicking noise up-converted to phase noise is mainly introduced by the tail current source. The low frequency noise and the even harmonic noise which came from the tail current source will be mixed and enter into the phase noise due to the mixing phenomenon of the differential pair transistor in the resonant.

The wide band nature of the resistor R_1 in the figure 2 can suppress the second harmonic as well as other even harmonics leaking from the LC tank, and avoid the high frequency harmonic mixing with the low frequency noise from the tail current source.

In MOS transistor, the output noise current increases in proportional to the square of trans-conductance. Generally, VCO generates a large signal swing which leads to large trans-conductance variation. Thus, the large signal swing may generate excess flicking noise current in the VCO, and this will be up-converted into the $1/f^3$ part of the phase noise. The $1/f^3$ corner frequency can be defined as follows:

$$\omega_{1/f^3} \approx \omega_{1/f} \cdot \left(\frac{c_0}{c_1}\right)^2 = \frac{K}{C_{ox}WL} \cdot \frac{g_m^2}{\gamma \cdot g_{d0}} \cdot \frac{1}{4kT} \cdot \left(\frac{c_0}{c_1}\right)^2 \qquad (3)$$

where g_m is the trans-conductance of the FET. We can reduce the $1/f^3$ corner frequency by restrain the trans-conductance of the transistor.

If we induce a damping resistor in the source of the FET such as figure 2, we can make the trans-conductance have a small change during a large voltage swing so that the output noise current has a relatively lower increasing speed. However, the inherent noise of the resistor would up-convert to the $1/f^2$ part of the phase noise. Thus we should trade off this complication and confirm the proper resistor value. In the proposed VCO, R_1 , R_2 , R_3 , R_4 and R_5 were chosen to be 110 Ω and 50 Ω respectively.The simulated results of the different VCOs were shown in figure3 and figure 4.

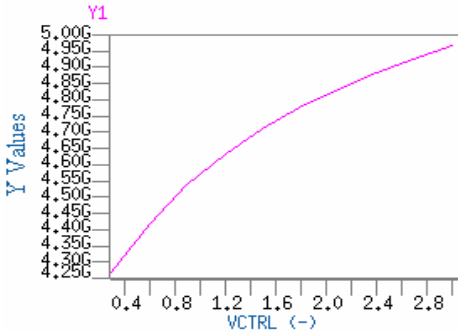

Figure 3 The range of the output frequency

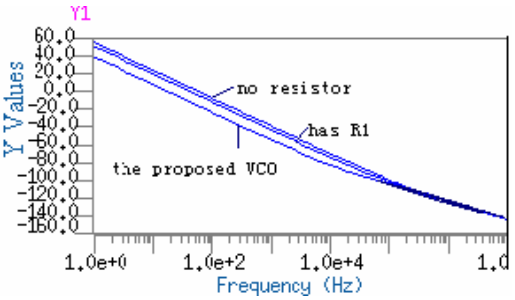

Figure 4 The simulation result of the phase noise

IV. RESULTS AND DISCUSSION

Generally, it's hard to compare the performance of the different oscillator, a formula being used regularity defined as follows [3]:

$$FOM = -L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P}{mW}\right) \qquad (4)$$

where f_0 is the centre frequency of the oscillator. Δf is the offset frequency where the phase noise was measured. $L(\Delta f)$ is the phase noise at the Δf , P is the DC power dissipation of the oscillator. The comparative results are shown in table 1.

TABLE I. THE COMPARATIVE RESULTS

Data resource	process	Δf (Hz)	P_{DC} (mW)	Phase noise (dBc/Hz)	f_0 (GHz)	FOM (dB)
[6]	0.24um CMOS	1M	5	-112	5.8	-180
[7]	0.18um CMOS	1M	8.1	-110	5.8	-176
[8]	------	1M	13.5	-124	5.3	-187.2
This Letter	0.35um CMOS	1M	7.09	-124.9	4.6	-189.65

V. CONCLUSION

The proposed VCO can restrain the flicking noise up-converter by the filtering resistor and restrain the noise current of the transistor itself by the source damping resistors so as to optimize the whole performance of the VCO and implemented a 4.6GHz VCO in the end. The proposed VCO can reach a phase noise of -124.9dBc/Hz at 1MHz offset while working from 4.15GHz to 5.0GHz in a 3mA excursion current during the 0 to 3 controlled voltage, the power consumption is only 7.09mW.

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