Dynamical analysis and experimental verification of valley current controlled buck converter*

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The dynamical behaviours of valley current controlled buck converter are studied by establishing its corresponding discrete iterative map model in this paper. Time-domain waveforms and phase portraits of valley current controlled buck converter are obtained by Runge–Kutta algorithm through a piecewise smooth switching model. The research results indicate that the valley current controlled buck converter exhibits rich nonlinear phenomena, and it has routes to chaos through period-doubling bifurcation and border-collision bifurcation in a wide parameter range. Interesting inverse nonlinear behaviours compared with peak current controlled buck converter are observed in the valley current controlled buck converter. Analysis and simulation results are verified by experimental results.

Keywords: buck converter, bifurcation, dynamical behaviour, iterative map
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1. Introduction

Switching dc–dc converters are composed of strong nonlinear circuits with rich nonlinear phenomena, such as sub-harmonic oscillations,[1] low frequency oscillation,[2−4] reducing frequency phenomenon,[5] period-doubling bifurcation,[6−9] border-collision bifurcation,[10−12] Hopf bifurcation,[13] time bifurcation,[14] complex intermittency, chaos[15,16] and so on. These nonlinear behaviours have great effects on the performances of switching dc–dc converters and have been investigated extensively in recent years.

The current-mode control technique, including peak current control, average current control, and valley current control, is one of the most widely applied control techniques for switching power converters. Among them, peak current control[8,11,12,17−20] and average current control[21] have been widely applied to the control of switching power converters and power–factor–correction (PFC) converters,[20,21] and the nonlinear phenomena and the dynamical behaviours of peak current controlled and average current controlled switching dc–dc converters and PFC converters have been extensively studied.

Valley current control technique of switching dc–dc converters was proposed recently[22] and found to have more and more applications to the design of switching dc–dc converters due to its very fast transient response. However, no research work has been reported on the nonlinear phenomena and dynamical behaviours of valley current controlled switching dc–dc converters or PFC converters so far. Therefore, it is necessary to study the nonlinear phenomena and dynamical behaviours of switching dc–dc converters with valley current control.

In this paper, by establishing a discrete iterative map model, the dynamical behaviours of valley current mode controlled buck converter operating in continuous conduction mode (CCM) are investigated in detail. Numerical and experimental results of time-domain waveform and phase portrait are given to verify the analysis results.

2. Discrete iterative map model of valley current controlled buck converter

Figure 1 shows the schematic of a valley current controlled buck converter, where power switch

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S_1, diode S_2, inductor L and capacitor C are all assumed to be ideal. The switch S_1 is turned off at the beginning of each switching cycle, i.e. at $t = nT$, with T being the switching period. Once the switch S_1 is turned off, the inductor current i_L will decrease linearly until it reaches the reference current I_{ref}. The switch S_1 is turned on when $i_L = I_{ref}$ and will remain in turn-on state until the end of this switching cycle.

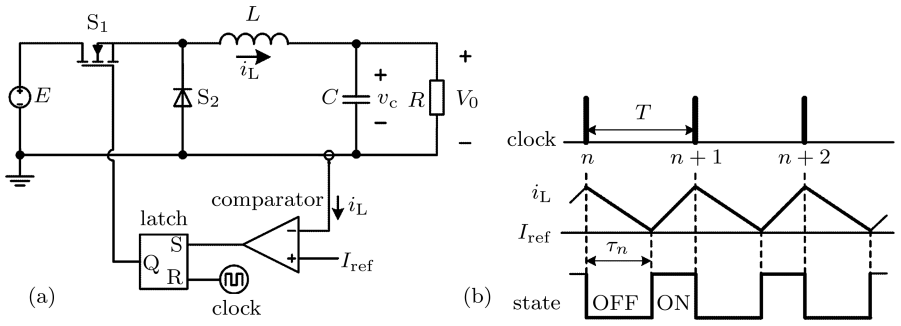

Fig. 1. Valley current controlled buck converter: (a) circuit schematic diagram; (b) operation waveforms.

Compared with peak current controlled buck converter where peak inductor current is taken as a control objective,[8,11,12,17–19] valley inductor current is taken as a control objective for valley current controlled buck converter. As the minimal value of I_{ref} is zero and whenever the inductor current i_L ramps down to I_{ref}, the switch S_1 will be turned on and inductor current will ramp up, valley current controlled buck converter cannot operate in discontinuous conduction mode. Therefore, the inductor current i_L never falls to and remains at zero and valley current controlled buck converter is kept working in CCM.

In Fig. 1, consider inductor current i_L and capacitor voltage v_c as state variables, the linear differential equations of valley current controlled buck converter during turn-on and turn-off states of the switch S_1 can be obtained.

During the turn-off state of the switch S_1, we have

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = -\frac{1}{L}v_c, \tag{1}$$

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = \frac{1}{C}i_L - \frac{1}{RC}v_c, \tag{2}$$

and during turn-on state of the switch S_1, we have

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{1}{L}E - \frac{1}{L}v_c, \tag{3}$$

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = \frac{1}{C}i_L - \frac{1}{RC}v_c. \tag{4}$$

To obtain the map model of switching dc–dc converters, the most widely used discrete-time map of switching dc–dc converters is adopted,[11,12,17–18] i.e. i_L and v_c are periodically sampled at time instants, $t = nT$. Let the initial conditions of state variables at the beginnings of the n-th and the $(n+1)$-th switching cycles be denoted as i_n, v_n and i_{n+1}, v_{n+1} respectively. As the switch S_1 is turned off at the beginning of each switching cycle and turned on when i_L decreases to I_{ref}, the turn-off time duration τ_n of the n-th switching cycle can be obtained from Eq. (1) as

$$\tau_n = \frac{L}{v_n}(i_n - I_{ref}). \tag{5}$$

To ensure CCM operation and low output voltage ripple,[23] the parameters of the buck converter usually satisfy $L < 4R^2C$. The capacitor voltage at $t = nT + \tau_n$ is thus obtained by solving Eqs. (1) and (2) as

$$v_c(\tau_n) = \mathrm{e}^{-\alpha\tau_n}\left[v_n\cos(\omega\tau_n) + \left(\frac{1}{\omega C}i_n - \frac{\alpha}{\omega}v_n\right)\sin(\omega\tau_n)\right], \tag{6}$$

where $\alpha = 1/2RC$ and $\omega = \sqrt{1/LC - \alpha^2}$.

The discrete iterative map model of valley current controlled buck converter can be derived in the following two cases: $\tau_n \geq T$ and $\tau_n < T$.

Case 1 $\tau_n \geq T$. The switch S_1 will remain in turn-off state throughout the switching cycle, and the iterative map in this case is given by

$$i_{n+1} = \mathrm{e}^{-\alpha T}\left[i_n\cos(\omega T) + \left(\frac{\alpha}{\omega}i_n - \frac{1}{\omega L}v_n\right)\sin(\omega T)\right], \tag{7}$$

$$v_{n+1} = \mathrm{e}^{-\alpha T}\left[v_n\cos(\omega T) + \left(\frac{1}{\omega C}i_n - \frac{\alpha}{\omega}v_n\right)\sin(\omega T)\right]. \quad (8)$$

Case 2 $\tau_n < T$. It means that i_{L} will decrease to I_{ref} and then increase until the end of the switching cycle. The iterative map in this case is given by

$$i_{n+1} = \mathrm{e}^{-\alpha(T-\tau_n)}[c_1\cos(\omega(T-\tau_n)) + c_2\sin(\omega(T-\tau_n))] + E/R, \quad (9)$$

$$v_{n+1} = \mathrm{e}^{-\alpha(T-\tau_n)}[c_3\cos(\omega(T-\tau_n)) + c_4\sin(\omega(T-\tau_n))] + E, \quad (10)$$

where

$$c_1 = I_{\mathrm{ref}} - \frac{E}{R}, \quad c_2 = \frac{\alpha}{\omega}c_1 + \frac{E - v_{\mathrm{c}}(\tau_n)}{\omega L},$$

$$c_3 = v_{\mathrm{c}}(\tau_n) - E, \quad c_4 = \frac{\alpha}{\omega}c_3 + \frac{I_{\mathrm{ref}} - v_{\mathrm{c}}(\tau_n)/R}{\omega C}.$$

Thus, the discrete iterative map model is composed of Eqs. (7)–(10), upon which the dynamical behaviours with the variation of circuit parameters of valley current mode controlled buck converter operating in CCM can be effectively exhibited.

Furthermore, it can be seen that there is an inductor current border in the discrete state-space for buck converter operating in CCM. The inductor current border I_{b} is defined as the value of inductor current at the beginning of the switching cycle which reaches I_{ref} just at the end of the switching cycle, based on which, the inductor current border, I_{b}, can easily be obtained from Eq. (7) as follows:

$$I_{\mathrm{b}} = \frac{I_{\mathrm{ref}}\,\mathrm{e}^{\alpha T} + v_n\sin(\omega T)/(\omega L)}{\cos(\omega T) + (\alpha/\omega)\sin(\omega T)}. \quad (11)$$

3. Bifurcation routes via period-doubling and border collision

When circuit parameters $E = 12$ V, $I_{\mathrm{ref}} = 0.6$ A, $C = 200$ μF, $L = 0.6$ mH, and $T = 50$ μs are keep constant while circuit parameter R is varying from 4 Ω to 10 Ω, the bifurcation diagram of the inductor current and the corresponding Lyapunov exponent of valley current controlled buck converter are obtained and shown in Figs. 2(a) and 2(b). Here, by the same idea as that in Ref. [9], the first Lyapunov exponent is given to verify the bifurcation diagram in this paper. To avoid presenting redundant results, only the first Lyapunov exponent is presented. It is clear that the bifurcation diagram well coincides with the first Lyapunov exponent. As R increases in the parameter variation range, two reverse bifurcation routes to chaos exist in valley current controlled buck converter.

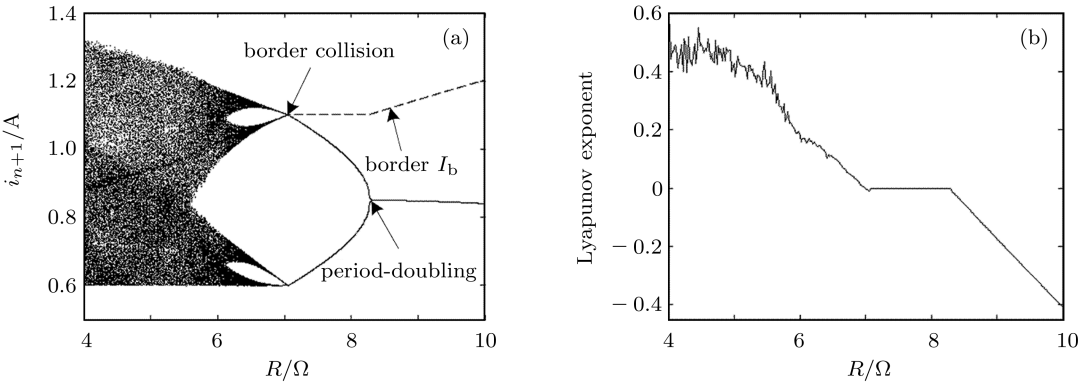

Fig. 2. Bifurcation diagram and first Lyapunov exponent versus R: (a) bifurcation diagram; (b) first Lyapunov exponent corresponding to (a).

As observed from Figs. 2(a) and 2(b), as parameter R gradually decreases, the first period-doubling bifurcation occurs at $R = 8.28$ Ω while the first Lyapunov exponent just reaches zero from a negative value at the same parameter value. After the first period-doubling bifurcation occurs, the buck converter operates with an unstable period-2 orbit. As parameter R further decreases, the border collision bifurcation occurs at $R = 7.06$ Ω since the unstable period-2 orbit collides with the borderline I_{b} separating two smooth regions, and the first Lyapunov exponent just turns into positive value simultaneously. Following the border collision, a chaotic orbit develops, and with further reducing the load resistance the pieces of the

attractor are joined pairwise into a one-piece attractor at about $R = 5.62\ \Omega$.

Corresponding to Fig. 2(a), the chaotic attractor with $R = 6\ \Omega$ and period-2 limit cycle with $R = 7.2\ \Omega$ of valley current controlled buck converter are shown in Figs. 3(a) and 3(b) respectively. In Fig. 3(a), two pieces of the chaotic attractor on the Poincaré section are visualised, which denotes that the buck converter has two attraction basins for chaotic orbit. While two dots on the Poincaré section are found in Fig. 3(b), which implies that the buck converter oscillates with period-2 subharmonic.

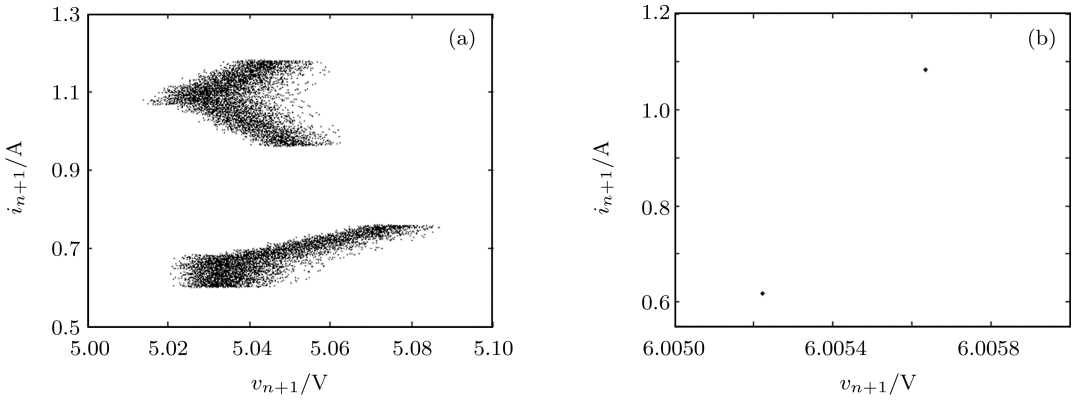

Fig. 3. Two Poincaré sections at different load resistances: (a) chaotic attractor with $R = 6\ \Omega$; (b) period-2 limit cycle with $R = 7.2\ \Omega$.

Figures 4(a) and 4(b) show the bifurcation diagrams of valley current controlled buck converter by taking input voltage E and reference current $I_{\rm ref}$ as bifurcation parameters respectively. From Figs. 4(a) and 4(b) we can know that the first period-doubling bifurcations occur at $E = 8.2$ V and $I_{\rm ref} = 0.88$ A respectively, while the border collision bifurcations happen at $E = 9.6$ V and $I_{\rm ref} = 0.75$ A respectively. As parameter E increases, forward bifurcation routes with period-doubling and border collision to chaos exist in this buck converter. While as parameter $I_{\rm ref}$ increases, reverse bifurcation routes with period-doubling and border collision to chaos then appear in this buck converter.

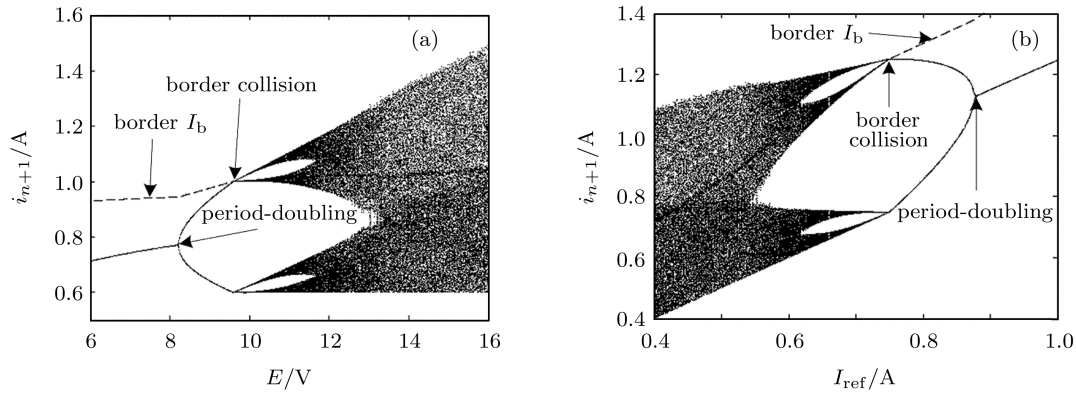

Fig. 4. Bifurcation diagram versus E and $I_{\rm ref}$: (a) $E = 6$–16 V; (b) $I_{\rm ref} = 0.4$–1 A.

Compared with the peak current mode controlled buck converter,[17,18] the valley current mode controlled buck converter has inverse bifurcation routes to chaos under the variation of circuit parameters.

4. Numerical and experimental verifications by time-domain waveform and phase portrait

The time-domain waveforms and the phase portraits are particularly important for observing nonlinear phenomena. By using Runge–Kutta algorithm via constructing piecewise smooth switching models of Matlab,

simulation results of the time-domain waveforms and the phase portraits (inductor current versus output voltage) for the valley current controlled buck converter can be obtained.

Taking the variation of load resistance into consideration, the time-domain inductor current waveforms for load resistances of 10 Ω, 7.2 Ω, and 5 Ω are shown in Figs. 5(a), 5(c), and 5(e), and their corresponding phase portraits are shown in Figs. 5(b), 5(d), and 5(f), which correspond to period-1 orbit, period-2 orbit, and chaotic orbit, respectively. The simulation results well coincide with the results shown in Fig. 2 obtained by using the discrete iterative map model.

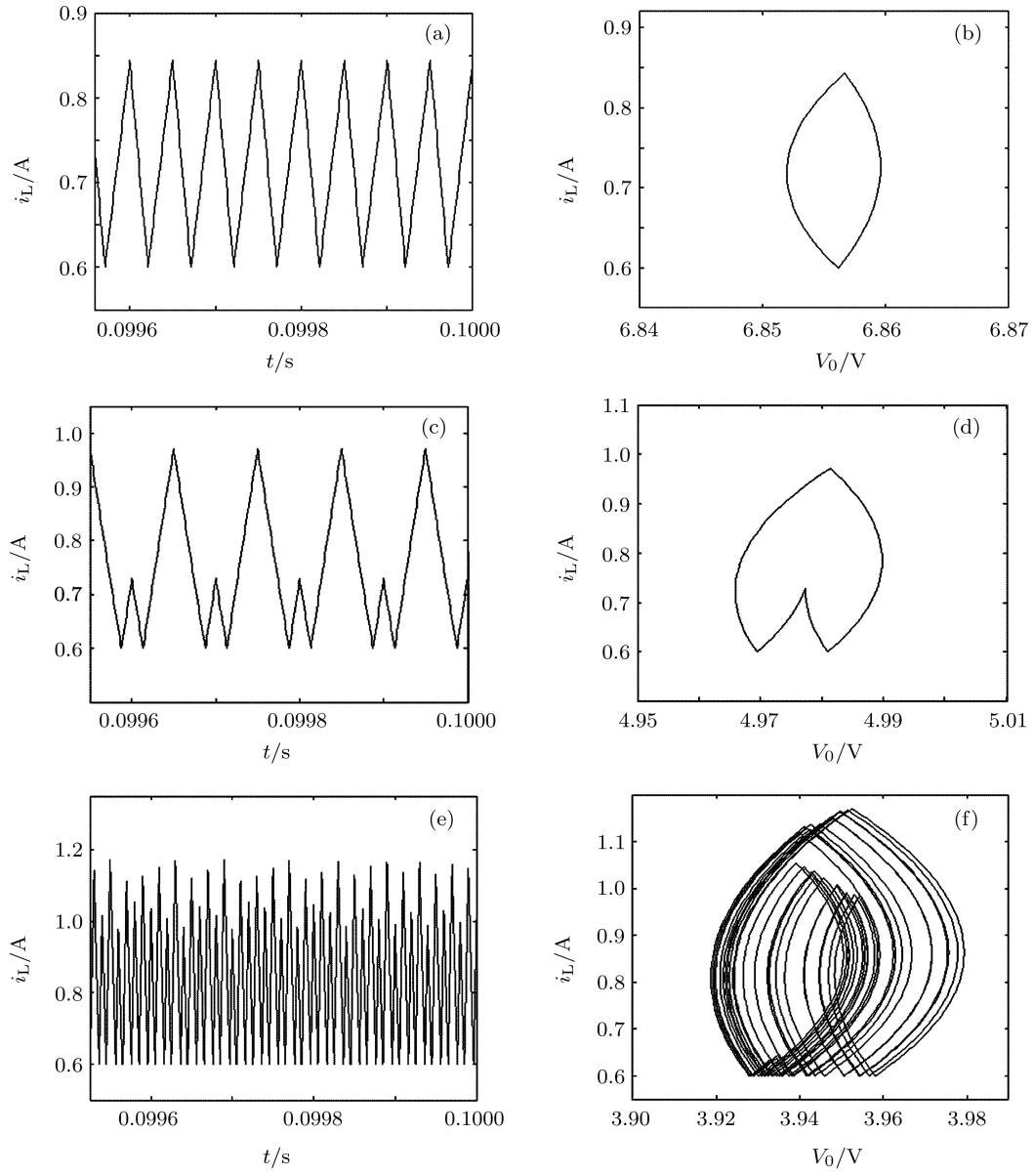

Fig. 5. Simulation time-domain waveforms and phase portraits of valley current controlled buck converter: (a) inductor current with period-1 orbit for $R = 10$ Ω; (b) phase portrait corresponding to (a); (c) inductor current with period-2 orbit for $R = 7.2$ Ω; (d) phase portrait corresponding to (c); (e) inductor current with chaotic orbit for $R = 5$ Ω; (f) phase portrait corresponding to (e).

To verify the analysis results and the simulation results discussed above, experimental prototype of valley current controlled buck converter is implemented, with the same circuit parameters as those used in the simulation. Figure 6 shows the experimental results with period-1 orbit, period-2 orbit, and chaotic orbit, which are in good agreement with simulation results shown in Fig. 5.

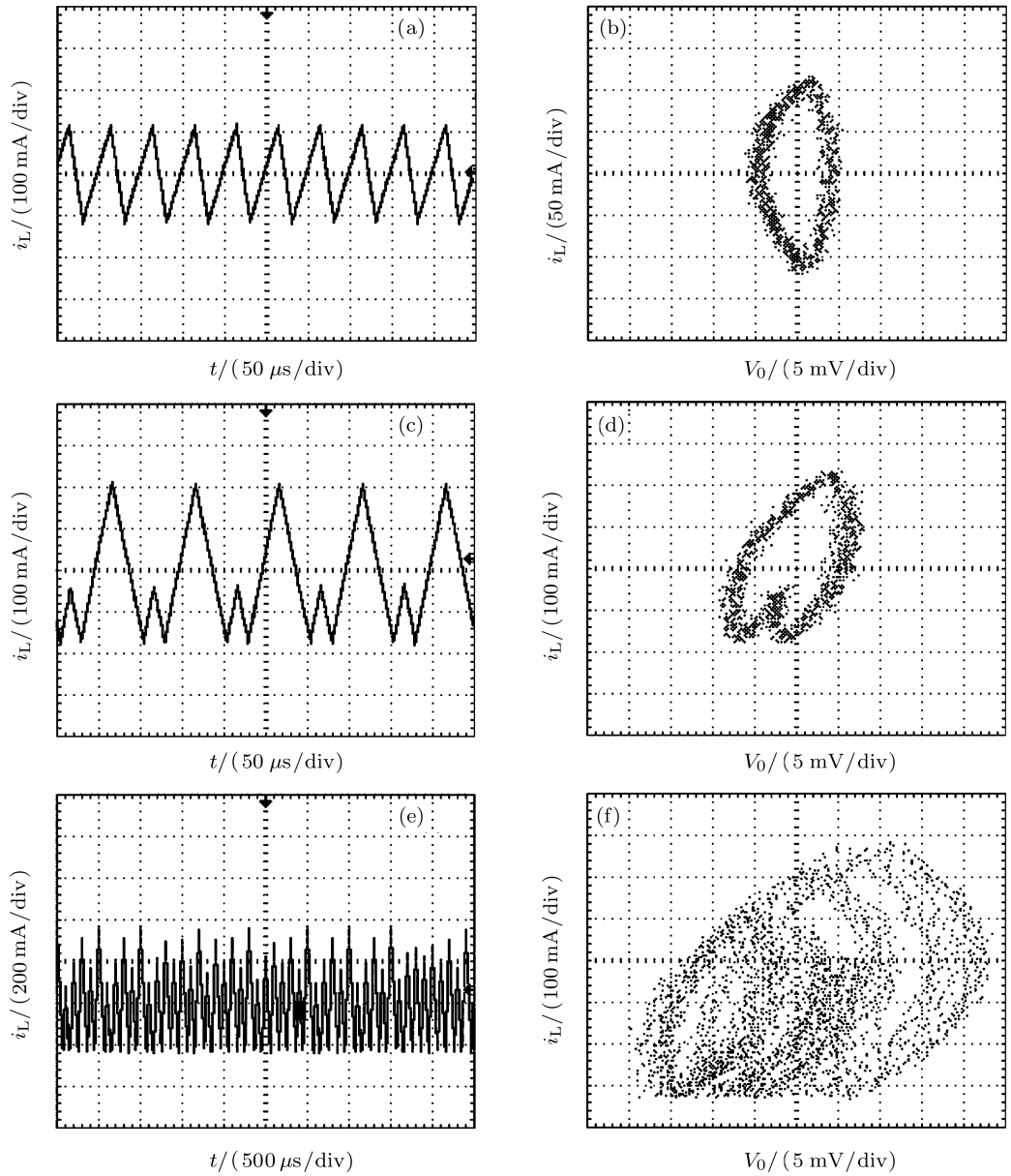

Fig. 6. Experimental results: (a) inductor current in period-1 orbit; (b) phase portrait corresponding to (a); (c) inductor current in period-2 orbit; (d) phase portrait corresponding to (c); (e) inductor current in chaotic orbit; (f) phase portrait corresponding to (e).

5. Conclusions

In this paper, we present a discrete iterative map model for valley current controlled buck converter, based on which, the dynamical behaviours with the variations of load resistance, input voltage and reference current are investigated by utilising conventional bifurcation analysis methods. With the variation of circuit parameters, the buck converter goes to chaos via period-doubling and border collision routes. Simulation results of bifurcation diagrams, Lyapunov exponent, Poincaré sections, time-domain waveforms, and phase portraits show that the valley current controlled buck converter exhibits a wide range of nonlinear behaviours. Especially, valley current controlled buck converter exhibits inverse nonlinear behaviours compared with peak current controlled buck converter. Experimental results are also given to verify the simulation results in this paper.

References

[1] Cafagnad D and Grassi G 2006 *Nonlinear Dynamics* **44** 251

[2] Maity S, Tripathy D, Bhattacharya T K and Banerjee S 2007 *IEEE Trans. Circuit Syst.* I **54** 1120

[3] Wang F Q, Zhang H and Ma X K 2008 *Acta Phys. Sin.* **57** 1552 (in Chinese)

[4] Zhang X T, Ma X K and Zhang H 2008 *Acta Phys. Sin.* **57** 6174 (in Chinese)

[5] Wang F Q, Zhang H and Ma X K 2008 *Acta Phys. Sin.* **57** 2842 (in Chinese)

[6] Wang X M, Zhang B and Qiu D Y 2008 *Acta Phys. Sin.* **57** 2728 (in Chinese)

[7] Yang R, Zhang B and Zhu L L 2008 *Acta Phys. Sin.* **57** 2770 (in Chinese)

[8] Aroudi A E, Benadero L, Toribio E and Olivar G 1999 *IEEE Trans. Circuits Syst.* I **46** 1374

[9] Chan W C Y and Tse C K 1997 *IEEE Trans. Circuits Syst.* I **44** 1129

[10] Banerjee S, Parui S and Gupta A 2004 *IEEE Trans. Circuits Syst.* II **51** 649

[11] Bao B C, Xu J P and Liu Z 2009 *Acta Phys. Sin.* **58** 2949 (in Chinese)

[12] Bao B C, Xu J P and Liu Z 2009 *Chin. Phys.* B **18** 4742

[13] Mazumder S K, Nayfeh A H and Boroyevich D 2001 *IEEE Trans. Power Electron.* **16** 201

[14] Zhou Y F, Chen J N, Iu H H C and Tse C K 2008 *Int. J. Bifurc. Chaos* **18** 121

[15] Zhusubaliyev Z T, Soukhoterin E A and Mosekilde E 2003 *IEEE Trans. Circuits Syst.* I **50** 1047

[16] Wong S C, Tse C K and Tam K C 2004 *Int. J. Bifurc. Chaos* **14** 2971

[17] Bao B C, Xu J P and Liu Z 2008 *J. University of Electronic Science and Technology of China* **37** 397 (in Chinese)

[18] Banerjee S, Parui S and Gupta A 2004 *IEEE Trans. Circuits Syst.* II **51** 649

[19] Zhao Y B, Zhang D Y and Zhang C J 2007 *Chin. Phys.* **16** 933

[20] Ren H P and Liu D 2005 *Chin. Phys.* **14** 1352

[21] Orabi M and Ninomiya T 2003 *IEEE Trans. Ind. Electron.* **50** 1116

[22] Rossetti N and Sanders S R 2001 *Power Electronics Technology* **27** 50

[23] Banerjee S and Chakrabarty K 1998 *IEEE Trans. Power Electron.* **13** 252