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Modified pseudo-noise code regeneration method

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Abstract: A modified pseudo-noise (PN) code regeneration method is proposed to improve the clock tracking accuracy without impairing the code acquisition time performance. Thus, the method can meet the requirement of high accuracy ranging measurements in short time periods demanded by radio-science missions. The tracking error variance is derived by linear analysis. For some existing PN codes, which can be acquired rapidly, the tracking error variance performance of the proposed method is about 2.6 dB better than that of the JPL scheme (originally proposed by Jet Propulsion Laboratory), and about 1.5 dB better than that of the traditional double loop scheme.

Keywords: regenerative pseudo-noise (PN) ranging, chip tracking loop, tracking error variance, code acquisition time.

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1. Introduction

The regenerative pseudo-noise (PN) ranging is suitable for space missions requiring high ranging accuracy as well as deep-space applications, and several PN codes have been considered for the consultative committee for space data systems (CCSDS) standard on regenerative PN ranging [1–4]. When a PN code regeneration scheme is evaluated, two performances are usually concerned in terms of clock timing-jitter and code acquisition time [1–4]. The JPL scheme (originally proposed by Jet Propulsion Laboratory) is now generally used for PN code regeneration [1]. For existing regenerative PN codes, however, this scheme is not capable to attain precision clock tracking and short code acquisition time simultaneously. In this work, a modified method is proposed to reduce the clock timing-jitter without degrading the code acquisition time performance. Thus, the method can meet the requirement of high accuracy ranging measurements in short time periods demanded by radio-science experiments in inner planetary missions [1,3].

2. Description of PN code regeneration schemes

The reader is referred to [1–8] for a background of regenerative PN codes. Seven PN codes (JPL99(T1), T4/T4B, T2/T2B, and SS8/SS6) have been considered and studied for regenerative ranging, and each code is a composite sequence which is made up of several components including a clock component. The existing of the clock component makes these PN codes ensemble alternative $+1/-1$ sequences. Two parameters characterizing these codes are concerned in following analysis: one, denoted as p_{C_1}, is the cross-correlation factor between the clock component (C_1) and the ranging code [3,8], and the other, expressed as p_t, is the transition density defined as the ratio of the number of transition and the number of chips in a PN code sequence.

Traditionally, a double loop (DBL) structure was frequently used for PN code tracking [9]. For deep space applications, onboard code tracking capability for uplink is not essential because the ranging capability is mainly limited by downlink. For this reason, a simplified structure (i.e. the JPL scheme) was later presented and is now extensively used for ranging code regeneration [10−13], as illustrated in Fig. 1, which consists of a chip tracking loop (CTL), correlators and a downlink code combiner [1]. The CTL is used to recover the clock from the received ranging signal. It was designed to simplifying a data transition tracking loop (DTTL) since the regenerative PN code resembles an alternative $+1/-1$ sequence. In the phase detector of the CTL, the output of the mid-phase integrator is multiplied by the clock component sequence C_{1k} (alternative $+1/-1$ sequence) to provide the right correction of the loop. In the correlators, the received sequence is correlated with local replicas of all components for a period of time to recover the code sequence position. This period of time is called the code acquisition time, which is relative to the signal to noise ratio (SNR) condition and the required successful acquisition probability [4]. A dedicated lock detector uses the acquisition results to indicate the code lock status. Once the code is locked, the PN combiner outputs the regenerated ranging code combining the recovered components [1].

With the JPL structure, ranging codes with good clock tracking accuracy (such as JPL99) generally have poor

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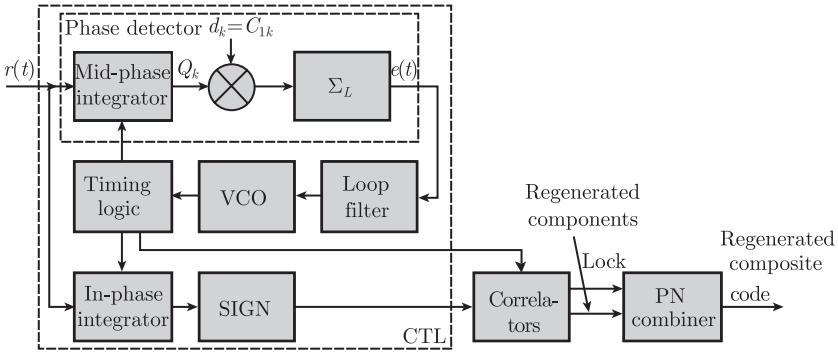

Fig. 1 The JPL structure

code acquisition performance, while those with fast code acquisition capability (such as T2/T2B) usually have inferior clock tracking performance [3−4]. This is not essential for deep space missions, but may become a thorny issue for radio-science missions which demands accurate and rapid PN code regeneration [1–3]. In particular, the T2 or T2B code (with the correlators involving 77 correlations per chip) is the only choice when rigorously short code acquisition time is required. However, their loop tracking error variances are too large compared with that of JPL99 [4], even though the DBL scheme is adopted [9]. To address this issue, a modified method is proposed as shown in Fig. 2, with only a slight increase in circuit compared with the JPL scheme. Initially, C_{1k} still serves as the correcting input of the phase detector. After the ranging code is locked, however, the regenerated composite sequence C_k is fed back to play the role instead so that every transition of C_k is used, which is similar to the DBL scheme. Moreover, the output of the mid-phase integrator is not accumulated unless a transition occurs in C_k ($C_k \neq C_{k-1}$) in order to decrease noise accumulation so that the loop timing-jitter is further reduced, which is different from DBL. Namely,

$$d_k = \begin{cases} C_{1k}\ (k\text{th chip of } C_1), & \text{before code lock} \\ C_k\ \ (k\text{th chip of } C), & \text{after code lock and } C_k \neq C_{k-1} \\ 0, & \text{after code lock and } C_k = C_{k-1} \end{cases} \tag{1}$$

Since the switch operation does not occur until the code is locked, the code acquisition time performance is not affected. The CTL loop status is not changed by the switch operation either, i.e. the loop is still in tracking. When the correlators lose lock on the received code, the correcting signal returns to being C_{1k}, and the system reenters the code acquisition phase.

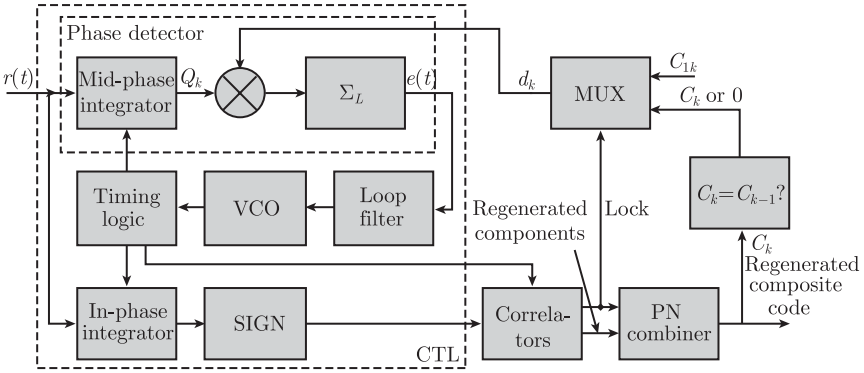

Fig. 2 The proposed structure

3. Performance analysis

The input of the CTL $r(t)$ is assumed to be a non-return-to-zero (NRZ) data stream plus additive white Gaussian noise (AWGN), which has the mathematical description as

$$r(t) = s(t,\varepsilon)+n(t) = A\sum_{m=-\infty}^{\infty} c_m h_{sq}(t-mT-\varepsilon)+n(t) \tag{2}$$

where $s(t,\varepsilon)$ is the signal component, A is the data signal amplitude, T is the chip time duration, c_m is the mth chip polarity, h_{sq} is a unit amplitude rectangular pulse in the interval $0 \leqslant t \leqslant T$, ε is the unknown chip timing epoch to be estimated, and the AWGN $n(t)$ has single-sided power spectral density N_0 (W/Hz). The output of the mid-phase integrator is

$$Q_k = \int_{(k-\frac{\xi}{2})T+\hat{\varepsilon}}^{(k+\frac{\xi}{2})T+\hat{\varepsilon}} s(t,\varepsilon)\mathrm{d}t +$$

$$\int_{(k-\frac{\xi}{2})T+\hat{\varepsilon}}^{(k+\frac{\xi}{2})T+\hat{\varepsilon}} n(t)\mathrm{d}t \triangleq b_k + N_k \tag{3}$$

where b_k is the signal components, $\hat{\varepsilon}$ is the estimated epoch, ξ is the window width of the mid-phase integrator, N_k is a Gaussian random variable with mean of zero and variance $\sigma_{N_k}^2 = \xi N_0 T/2$. For $k \neq l$, N_k and N_l are mutually independent. With $\lambda = (\varepsilon - \hat{\varepsilon})/T$ denoting the normalized timing error ($-1/2 \leqslant \lambda \leqslant 1/2$), b_k becomes

$$b_k = \begin{cases} AT[c_{k-1}(\xi/2+\lambda)+c_k(\xi/2-\lambda)], & 0 \leqslant \lambda \leqslant \xi/2 \\ ATc_{k-1}\xi, & \xi/2 \leqslant \lambda \leqslant 1/2 \end{cases} \tag{4}$$

Therefore, the loop error $e(t)$ can be expressed as

$$e(t) = e_i = \sum_{k=iL}^{(i+1)L-1} (Q_k \times d_k) = \sum_{k=iL}^{(i+1)L-1} [(b_k + N_k) \times d_k] \tag{5}$$

where L is the length of the accumulator shown in Figs. 1−2 and is large enough for practical applications, and d_k is defined as (1).

3.1 S-curve performance

The S-curve is by definition the statistical average of the error signal of (5) over the signal and noise probability distributions, i.e.

$$g(\lambda) = \mathrm{E}_{n,s}[e(t)] = \mathrm{E}_{n,s}\left[\sum_{k=iL}^{(i+1)L-1} [(b_k + N_k) \times d_k]\right] = \mathrm{E}_s\left[\sum_{k=iL}^{(i+1)L-1} (b_k \times d_k)\right] \tag{6}$$

where $\mathrm{E}_{n,s}(\cdot)$ denotes expectation over both signal and noise, and $\mathrm{E}_s(\cdot)$ represents expectation over signal. Using (1), substituting (4) into (6), and performing the necessary averaging over the chip symbols c_{k-1} and c_k result in the desired S-curve expression, namely

$$g(\lambda) = \begin{cases} g_1(\lambda) = 2p_{C_1}\lambda AT_u, \text{ JPL scheme} \\ g_2(\lambda) = 2p_t\lambda AT_u, \text{ modified scheme} \\ g_3(\lambda) = 2p_t\lambda AT_u, \text{ DBL scheme} \end{cases} \tag{7}$$

where $T_u = LT$ is the loop updating time interval.

The slope of the S-curve at the origin is

$$K_g = \begin{cases} K_{g_1} = 2p_{C_1}AT_u, \text{ JPL scheme} \\ K_{g_2} = 2p_tAT_u, \text{ modified scheme} \\ K_{g_3} = 2p_tAT_u, \text{ DBL scheme} \end{cases} \tag{8}$$

3.2 Noise performance

The equivalent additive noise in the loop is

$$n_\lambda(t) = e_i - \mathrm{E}_{n.s}(e_i) = e_i - g(\lambda) \tag{9}$$

As is customary in the analysis of loops of this type, for loop bandwidths which are small compared with the reciprocal of the chip time interval, it is sufficient to approximate the spectral density of $n_\lambda(t)$ at zero frequency, i.e.

$$N_0' = N_0'(0,\lambda) = \int_{-\infty}^{\infty} R_n(\tau)\mathrm{d}\tau = T_u\left[R(0,\lambda) + 2\sum_{j=1}^{\infty} R(j,\lambda)\right] \tag{10}$$

where N_0' is the power spectral density of the equivalent additive noise in the loop, and

$$R(j,\lambda) = \mathrm{E}[n_\lambda(t)n_\lambda(t+jT_u)] = \mathrm{E}_{n,s}(e_ie_{i+j}) - g^2(\lambda), \quad j = 0, \pm1, \pm2, \ldots \tag{11}$$

After some algebra, one can obtain

$$N_0' = \begin{cases} N_{01}' = \xi N_0 T_u^2/2, \text{ JPL scheme} \\ N_{02}' = p_t\xi N_0 T_u^2/2, \text{ modified scheme} \\ N_{03}' = \xi N_0 T_u^2/2, \text{ DBL scheme} \end{cases} \tag{12}$$

3.3 Mean-square timing-error performance

For large loop SNR, the linearized loop model can be used to derive the mean-square timing jitter performance for DTTL-like loops [14−15], i.e.

$$\sigma_\lambda^2 = (2N_0'B_L)/K_g^2 \tag{13}$$

where B_L is the single-sided loop bandwidth defined as

$$B_L = \int_0^{\infty} |H(\mathrm{j}2\pi f)|^2\mathrm{d}f \tag{14}$$

where $H(f)$ is the closed-loop transfer function of the linear equivalent model.

Substituting (8) and (12) to (13) results in

$$\sigma_\lambda^2 = \begin{cases} \sigma_{\lambda1}^2 = (\xi/4p_{C_1}^2)(B_LP_r/N_0), \text{ JPL scheme} \\ \sigma_{\lambda2}^2 = (\xi/4p_t)(B_LP_r/N_0), \text{ modified scheme} \\ \sigma_{\lambda3}^2 = (\xi/4p_t^2)(B_LP_r/N_0), \text{ DBL scheme} \end{cases} \tag{15}$$

where $P_r/N_0 = A^2T/N_0$ represents the ranging SNR. Consequently, the improvements of the tracking error variance are

$$\eta_1 = -10\mathrm{lg}\,(\sigma_{\lambda2}^2/\sigma_{\lambda1}^2) = -10\mathrm{lg}\,(p_{C_1}^2/p_t) \tag{16}$$

$$\eta_2 = -10\mathrm{lg}\,(\sigma_{\lambda2}^2/\sigma_{\lambda3}^2) = -10\mathrm{lg}\,p_t \tag{17}$$

4. Numerical and simulation results

According to (15)−(17), the computational performances of the seven typical codes are listed in Table 1, where $\sigma_{\lambda1}^{'2}$, $\sigma_{\lambda2}^{'2}$ and $\sigma_{\lambda3}^{'2}$ respectively represent the clock tracking error

variances of the JPL, the modified and the DBL schemes, all normalized by that of JPL99 with DBL (under the same conditions of ξ, B_L and P_r/N_0). $T'_{\rm acq}$ is the code acquisition time normalized by that of JPL99. Note that the $T'_{\rm acq}$ of JPL99, T4/T4B and T2/T2B are based on the correlators structure involving 77 correlations per chip, and that of SS8 and SS6 correspond to the structure of 4 parallel correlators [4]. As shown in Table 1, the acquisition time of T2 or T2B is the shortest, and is about 3% of JPL99. However, with the JPL scheme, their tracking error variances are too inferior, and are 3.78 dB and 3.64 dB worse than that of JPL99, respectively. Even though the DBL scheme is adopted, the tracking performances of T2 and T2B are still 2.69 dB and 2.55 dB worse than that of JPL99, respectively.

Table 1 Numerical results for typical ranging codes

Ranging codes	p_{C_1}	p_t	$\sigma'^2_{\lambda 1}/\sigma'^2_{\lambda 2}/\sigma'^2_{\lambda 3}$ /dB	η_1/η_2 /dB	$T'_{\rm acq}$
JPL99	0.954 4	0.954 4	0/-0.20/0	0.20/0.20	1
T4	0.933 8	0.936 6	0.18/-0.12/0.16	0.31/0.28	0.46
T4B	0.938 7	0.941 5	0.14/-0.15/0.11	0.29/0.26	0.53
T2	0.617 6	0.699 6	3.78/1.15/2.69	2.63/1.55	0.03
T2B	0.627 4	0.710 9	3.64/1.07/2.55	2.57/1.48	0.03
SS8	0.936 4	0.939 7	0.16/-0.14/0.13	0.30/0.27	4.87
SS6	0.832 9	0.861 0	1.18/0.24/0.89	0.94/0.65	1.04

In Table 1, it is clear that with the proposed method, the tracking performances of all ranging codes are more or less improved. The reason is that with the proposed method, the phase detector of the CTL not only effectively utilizes every transition of the ranging code sequence (shown as (8)), but also only uses these transitions avoiding excessive noise accumulation (shown as (12)). Mathematically,

$$p_{C_1} \leqslant p_t \ \text{ and } \ p_t < 1 \Rightarrow \eta_1 > 0, \eta_2 > 0 \qquad (18)$$

In addition, the T2 and T2B codes especially benefit from the proposed method. Their tracking error variances are 2.63 dB and 2.57 dB better than that of the JPL scheme, and 1.55 dB and 1.48 dB better than that of DBL, resulting in only 1.15 dB and 1.07 dB worse than that of JPL99 with DBL, respectively. However, for JPL99, the tracking performance is only improved 0.20 dB. This is reasonable since the proposed method is particularly beneficial to ranging codes with low p_t or with large difference between p_{C_1} and p_t, as implied in (16) and (17). Ranging codes of this type allocate relatively more power to the non-clock components, resulting in fast code acquisition. On the other hand, the clock tracking performance also becomes acceptable with the proposed method.

Above results are also demonstrated clearly in Fig. 3, where the curves of tracking error variance versus code transition density for the three loop structures are depicted, with the values for various ranging codes included as solid points on the curves.

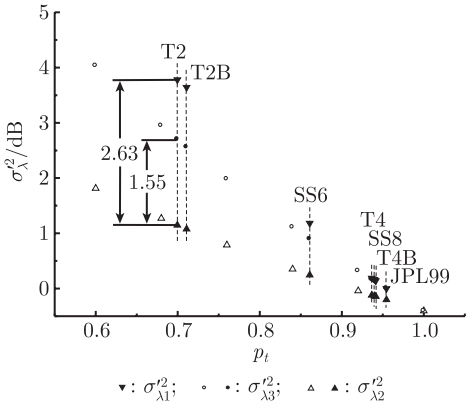

Fig. 3 Curves of tracking error variance versus code transition density for the JPL ($\boldsymbol{\sigma'^2_{\lambda 1}}$), the DBL ($\boldsymbol{\sigma'^2_{\lambda 3}}$), and the proposed schemes ($\boldsymbol{\sigma'^2_{\lambda 2}}$)

Simulation is performed to validate the theoretical results. The three schemes are simulated for comparison, and T2B is selected as an example code. The tracking error variance as a function of ranging SNR is plotted in Fig. 4, where a relatively high SNR region is involved since the work is motivated by precision ranging applications. It is shown that the tracking error variance of the proposed scheme is about 2.6 dB smaller than that of the JPL scheme, and about 1.5 dB smaller than that of DBL, which well accords with theory.

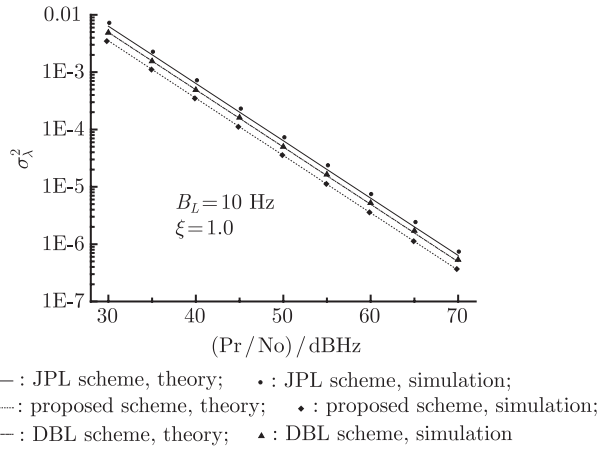

Fig. 4 Loop tracking error variance of the T2B ranging code

5. Conclusion

In this work, a modified PN code regeneration method is proposed to improve the clock tracking accuracy without jeopardizing the code acquisition time performance. The method is especially beneficial to ranging codes with low

p_t or with large difference between p_{C_1} and p_t, which also indicates an idea to devise new ranging codes with better ranging performance. In existing regenerative PN codes, T2 and T2B are superior in acquisition time performance. With the proposed method, their clock tracking variances are reduced by about 2.6 dB compared with that of the JPL scheme, and 1.5 dB compared with that of the DBL scheme. Therefore, the T2 or T2B ranging code can be recommended for future radio-science missions.

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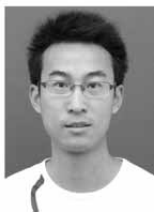

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