## A High Performance Silicon-on-Insulator LDMOSTT Using Linearly Increasing Thickness Techniques \*

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We present a new technique to achieve uniform lateral electric field and maximum breakdown voltage in lateral double-diffused metal-oxide-semiconductor transistors fabricated on silicon-on-insulator substrates. A linearly increasing drift-region thickness from the source to the drain is employed to improve the electric field distribution in the devices. Compared to the lateral linear doping technique and the reduced surface field technique, two-dimensional numerical simulations show that the new device exhibits reduced specific on-resistance, maximum off- and on-state breakdown voltages, superior quasi-saturation characteristics and improved safe operating area.

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Power metal-oxide-semiconductor field effect transistors (MOSFETs) have attraction much attention due to their determinant influence on properties of power integrated circuits.<sup>[1-3]</sup> Reduced surface field (RESURF) technology is commonly used to design power transistors on silicon-on-insulator (SOI) substrates for high voltage and high power applications.<sup>[3,4]</sup> However, sharp electric peaks at the ends of the drift region have been shown to result in low breakdown voltages.<sup>[5,6]</sup> A lateral linear doping profile in the drift region can be employed to improve the breakdown voltage by imposing a uniform lateral electric field distribution.<sup>[7,8]</sup> However, to maintain a high breakdown voltage, the doping concentration near the source side of the drift region must be kept small, thereby leading to a series of new problems, typically a large specific on-resistance resulting in conduction losses.



**Fig. 1.** Schematic of a new SOI LDMOST with a linear drift-region thickness.

To overcome the drawback of RESURF de-

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vices and linear doping (LD) devices having a lateral linear doping profile, in this Letter we propose a novel SOI lateral double-diffused metal-oxidesemiconductor transistor (LDMOST) with a linear thickness and a uniform doping concentration in the drift region. Figure 1 shows the proposed cross-sectional linear thickness (LT) LDMOST. The drift-region thickness increases continuously from the source side to the drain side while the doping concentration is kept uniform as in conventional RESURF devices. This means that the doping density (multiplying the doping concentration by the thickness) in the drift region maintains a linear function which is similar to that in an LD device.



Fig. 2. Breakdown voltage versus the average doping concentration in the drift region for LT, LD and RESURF devices.

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|   | Linear thickness    | Linear doping              | RESURF              |
|---|---------------------|----------------------------|---------------------|
| Top silicon layer thickness (µm)                    | 3 - 2.8x/L          | 3                          | 3                   |
| Buried oxide layer thickness $(\mu m)$              | 2.5                 | 2.5                        | 2.5                 |
| Drift region length $(\mu m)$                       | 15                  | 15                         | 15                  |
| Optimized drift doping concentration $(cm^{-3})$    | $7.1 	imes 10^{15}$ | $7.1(1-x/L) 	imes 10^{15}$ | $2.8 	imes 10^{15}$ |
| Maximized breakdown voltage (V)                     | 318                 | 316                        | 253                 |
| Specific on-resistance $(\Omega \cdot \text{mm}^2)$ | 1.37                | 2.13                       | 1.66                |
| Baliga's figure of merit $(kW \cdot mm^{-2})$       | 295.3               | 187.5                      | 154.2               |

Table 1. Key geometric parameters and performances of the investigated devices (L: drift-region length).



**Fig. 3.** Equipotential contours of the (a) LT, (b) LD and (c) RESURF devices at breakdown voltages (BVs).

MEDICI, a semiconductor simulation tool, is employed to investigate the breakdown performance of the novel device. Figure 2 compares the breakdown performances of the LT, LD and RESURF devices. The three devices have the same geometric parameters including top silicon layer thickness of  $3\,\mu\text{m}$ , buried oxide thickness of  $2.5\,\mu\text{m}$ , and driftregion length of 15 µm. The horizontal axis represents the average doping concentration defined by  $N_{av} = (1/L) \int_0^L N(x) dx$ , where L is the drift-region length, N(x) is the lateral doping profile in the drift region. The figure shows that the breakdown voltage can be maximized by adopting the optimum average doping concentration. Table 1 gives the optimum geometric and performance parameters of the three devices, The results show that the LT and LD devices present much better reverse-breakdown capacities than the conventional RESURF device. To investigate the underlying physics, Fig. 3 compares the equipotential lines of the three devices. As shown in Figs. 3(a) and 3(b), the LT and LD devices provide uniform potential distributions along the surface of the drift region which achieves almost uniform surface electric fields. In fact, to our knowledge, the linear thickness technique proposed here and the linear doping technique are the only solutions to obtain uniform

surface electric field and maximum lateral breakdown voltage in SOI power devices. Figure 3(c) shows that the conventional RESURF device causes severe crowding of the equipotential lines near the ends of the drift region, resulting in a sharp reduction in breakdown voltage.



**Fig. 4.** Breakdown voltage and specific on-resistance versus the drift shape factor with various drift doping concentrations: (a) breakdown voltage, (b) specific on-resistance.

Table 1 also shows another attractive characteristic of the LT device, i.e. its extremely low specific on-resistance. Compared with the conventional RESURF technique, the LT device reduces the specific on-resistance by 55% due to the higher (over two times) doping concentration in the drift region. However, the on-resistance of the LD device is 28% larger than that of the RESURF device because of the much lower doping concentration in the drift region near the channel side as mentioned above. Note that, although the shrink of the drift-region thickness near the channel tends to raise the specific on-resistance in the LT device, the results in Table 1 show that the increase of the doping concentration has a strongly compensating effect, thus leading to a minimum specific onresistance compared with the LD and RESURF devices. Figure 4 gives a more detailed investigation of the influence of drift-region thickness on the breakdown and conduction performances. The horizontal axis  $\gamma$  denotes a shape factor of the drift region and follows the expression  $\gamma = t_0/t_L$ , where  $t_0$  and  $t_L$  are the drift-region thicknesses at the channel and drain sides, respectively. For a fixed  $t_L$ , Fig. 4(a) shows that breakdown voltage increases with the reduction of  $t_0$ and with the increase of the doping concentration in the drift region. For the specific on-resistance, however, Fig. 4(b) shows that the reduction of  $t_0$  and increase of the drift doping concentration lead to opposite effects. In other words, the former increases the specific on-resistance while the latter decreases it more. As a result, the LT device exhibits the lowest specific on-resistance compared to the RESURF and LD devices.

Table 1 also compares the Baliga figure-of-merit (BFOM) values of the three devices.<sup>[9]</sup> It is evident that the LT device exhibits an excellent BFOM due to the best tradeoff between the breakdown voltage and on-resistance, which is over double that of the conventional RESURF device and 1.5 times that of the LD device.



Fig. 5. Drain-to-source currents versus drain voltages for various gate-biased voltages for the (a) LT, (b) LD and (c) RESURF devices.

The third benefit of the LT device is its superior safe operation area (SOA) due to the excellent conduction characteristics. Figure 5 illustrates the drain voltage-current curves of the LT, LD and RESURF devices for a series of gate bias voltages. Firstly, the LT device explores a high second breakdown voltage. The reason for this is that the second breakdown voltage presents a linearly increasing trend with the increase of the off-state breakdown voltage despite the different insight physics. Secondly, in the RESURF and LD devices, the evident quasi-saturation effect can be observed when the gate voltage approaches 5 V. As shown in Fig. 5(a), however, the quasi-saturation phenomenon in the LT device is still indistinct until the gate voltage exceeds 7 V. A heavy doping level and variable drift-region thickness in the LT device cause the reduced lateral electric fields and high internal drain voltages, [10,11] as shown in Fig. 6, which means that consequently carrier velocity saturations in the drift region are suppressed and the quasi-saturation effect is postponed until a higher gate-biased voltage is applied.<sup>[12]</sup> To sum up, the increasing second breakdown and quasi-saturation performances in the LT device can cause a higher input voltage level and a larger output current level, respectively. Thus an excellent SOA is exhibited.



Fig. 6. Internal drain potentials of the LT, LD and RESURF devices versus the gate voltage for the fixed drain voltage and grounded source and substrate.



**Fig. 7.** Static-potential distribution at breakdown based on process-device co-simulation.

It should be pointed out that the biggest challenge to integrate a novel LT device into a monolithic integrated circuit with other logic and analog devices is the fabrication of a linearly-increasing drift-region thickness on the SOI substrate. The practical candidate methods are oxidation or anisotropic-etching under an additional mask with a series of sequential openings of different widths.<sup>[13,14]</sup> A process and device co-simulation result based on TSUPREM4 and MEDICI is shown in Fig. 7. The static-potential distribution in the figure shows that the proposed LT device has a uniform electric field in the drift region. Its breakdown voltage of 312 V is very close to the ideal result shown in Table 1 and Fig. 2. Due to the limitation of the paper length, a detailed investigation of the fabrication method and its influence on operating reliability will be reported elsewhere.

In conclusion, a novel technique for high performance SOI high voltage LDMOST devices is proposed. Unlike conventional RESURF and linear doping technologies, the new device uses a drift region with linearly-increasing thickness to improve the lateral electric field distribution in the drift region. Such a technique gives a new approach to achieve a uniform lateral electric field in the SOI high voltage device. Numerical simulation using MEDICI tools shows that LDMOSTTs with the technique exhibit a superior operation performance in terms of maximum offand on-state breakdown voltages, minimum attainable specific on-resistance, large BFOM value, larger operation current-flow, increasing quasi-saturation effect, high conductional current flow levels and improved SOA.

## References

- Zhang T, Lu H L, Zhang Y M, Zhang Y M and Ye L H 2008 Chin. Phys. Lett. 25 1818
- [2] Yang F, Jin K J, Lu H B, He M and Yang G Z 2009 Chin. Phys. Lett. 26 077301
- [3] Qiao M, Zhang B, Li Z J and Fang J 2007 Electron. Lett. 43 1231
- [4] Huang Y S and Baliga B J 1991 Proceedings of International Symposium on Power Semiconductor Devices and ICs (Baltimore, USA 22-24 April 1991) p 27
- [5] Cheng J B, Zhang B, Duan B X and LI Z J 2008 *Chin. Phys. Lett.* **25** 262
- [6] Guo Y F, Li Z J and Zhang B 2006 Microelectron. J. 37 861
- [7] Merchant S, Arnold E, Baumgart H, Pein H and Pinker R 1991 Proceedings of International Symposium on Power Semiconductor Devices and ICs (Baltimore, USA 22-24 April 1991) p 31
- [8] Zhang S D, Sin J K O and Laim T M L 1999 IEEE Trans. Electron. Devices 46 1036
- [9] Baliga B J 1989 IEEE Electron. Device Lett. 10 455
- [10] Darwish M N 1999 IEEE Trans. Electron. Devices 44 1117
- [11] Aarts A C T and Kloosterman W J 2006 IEEE Trans. Electron. Devices 53 897
- Baliga B J 1995 Power Semiconductor Devices (Boston: PWS) chap 7 p 335
- [13] Letavic T and Simpson M 2001 US Patent 6221737B1
- [14] Monteiro D W, Akhza L O, Sarro P M and Vdovin G 2003 Opt. Express 41 2244