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A High-Efficiency Work-on-Demand SoC with a 0.9V/165μW MCU and Dual-Band RF for WBSN*

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Abstract — An SoC with a 0.9V/165μW MCU and dual-band RF is presented for Wireless body sensor networks (WBSN). The SoC contains a 403MHz transceiver and a 915MHz receiver, of which the 403MHz band is composed of a 200kbps FSK transmitter and a 64kbps OOK receiver, consuming 5.58mW and 3.13mW, respectively. The 915MHz receiver based on energy harvesting gives the SoC the unique high-efficiency work-on-demand capability, avoiding wasting energy during the idle-listening period. The power consumption of the integrated MCU is only 1/3 of the previous SoC designs in WBSN applications, implementing the on-demand MAC protocol with instant response, satisfying the requirements of medical WBSN applications.

Key words — Work on demand, Low power, SoC, Wireless body sensor networks (WBSN).

I. Introduction

Recently, the emerging Wireless body sensor networks (WBSN) become more and more attractive in pervasive healthcare and medical care applications such as vital signs monitoring, diagnose assistant, and drug delivery[1−3].

A typical WBSN adopts single-hop star topology and master-slave protocol, containing a Base station (BS) and a set of implantable/wearable sensor nodes for various vital sign sensing. The sensor devices are placed around, on or in the human body. The sensor nodes play a more crucial role because they suffer from much more critical design constraints. Miniature and low power features are required to avoid harm to the human body, to achieve unobtrusive, minimal interventions and long lifetime, *etc.*

The sensor nodes are mainly designed for two purposes, health monitoring and basic medical treatment[4]. The Monitoring function (MF) nodes are generally used for information acquisition, pre-processing, storage and transmission (maybe raw data without pre-processing); while the Treatment function (TF) nodes are used to deliver drug or output stimulus, *etc.* The major difference between the two types of nodes is: MF requires "time-driven", while TF prefers "event-driven". It is important to find an efficient scheme and architecture for these nodes.

For communication links between the BS and the sensor nodes, the "idle-listening" operations consume the highest energy[5]. However, for those WBSNs with only burst data link initiated by the BS side, the sensor nodes are required to work in the idle-listening mode for most of its lifetime. The idle-listening can be continuous or periodical. Continuous listening can guarantee that the sensor node responds to the BS promptly, namely "works on demand", but is not energy efficiently. There always exists a tradeoff between low-power and instant response channel monitoring[6] in common implementations, because in their half-duplex single-channel configuration, periodical listening can help to save power, but consequently lose the capability of instant network response. In this work, the sensor node architecture with a hybrid of passive/active RF transceivers is proposed to solve this problem. Each sensor node only needs an extra receiver for the simplex behavior (only listen function) in a "secondary" channel. By utilizing the passive RF module, the event-driven nodes do not need to consume battery energy in channel listening any more.

In this paper, a sensor node SoC with a 0.9V/165μW MCU and dual-band RF which is uniquely featured with continuous but high-efficient listening is presented. A power management module is designed to co-operate with the hybrid architecture of active/passive RFs. It contains several optional power-saving schemes, of which the highest saving method can shut down all the analog modules to eliminate quiescent current when needed. The digital core of the designed ASIC is mainly utilized to accomplish all the network protocols and MAC control for both primary/ secondary channels. Other Ultra-low-power (ULP) design techniques are utilized such that SoC represents state-of-the-art in terms of overall power consumption.

This paper is organized as follows. Section II reviews the fundamental concepts. Section III shows the proposed architecture. Section IV illustrates the implementations. Section

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V gives the verification and test results.

II. Fundamental Concepts

As stated above, the hardware developed in this work is for the healthcare and medical care applications. This section discusses the basic requirements of medical WBSN.

1. Typical WBSN: BS & sensor nodes

Fig.1 shows some typical applications in WBSN. The architecture of WBSN is divided into two major parts: the BS and the sensor nodes. This topology brings low complexity and lower power consumption compared with complicated peer-to-peer self-organized network topologies. The sensor nodes are usually battery-powered, small encapsulated and low cost. The small size of sensor node also limits the battery volume, so low power techniques are adopted to prolong the battery lifetime, *e.g.* power gating, clock gating, voltage scaling, *etc.*

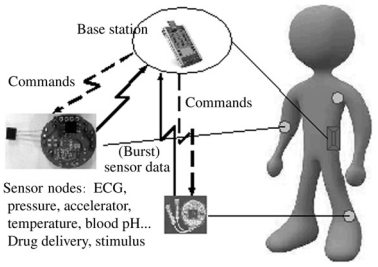


Fig. 1. System diagram of typical WBSN applications

At system level, there are 2 states for a certain sensor node: work and idle, as shown in Fig.2(a). In working state (T_{work}), the node is activated to perform data acquisition or transmission operations, etc. Fig.2(b) zooms in T_{work} duration. Each working phase requires different modules to be enabled. Fig.2(c) gives a more specific example of MCU: not all modules inside MCU are enabled after system activated, but only some interface controllers enabled in phase I, memory and ALU enabled in phase II, *etc.*

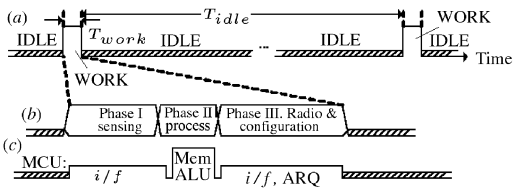


Fig. 2. (a) states; (b) work state; (c) MCU power of sensor nodes

2. MF and TF nodes

In WBSN, the MF nodes mainly work in a way of low duty cycle and act as "in-vivo information collector", which normally work periodically to sense/communicate. (*e.g.* glucose detector activates every 5 min); TF nodes mainly feedback stimulus to the human body whenever it is necessary, *e.g.* insulin delivery operation occurs due to glycemia detected.

A possible procedure of a typical medical WBSN is:

(1) MF nodes become activated after an idle interval, periodically.

(2) Once MF nodes detected abnormity, emergency requests are transmitted up to the BS.

(3) The BS wakes the relevant TF node up.

(4) TF node performs operations requested by the BS.

Consequently, the time-driven schedules are qualified for MF nodes monitoring: only a timer is required during the idle intervals between consecutive working states.

However, TF nodes should be event-driven instead of time-driven because they hold in idle state for almost entire of lifetime. The tradeoff between energy efficiency and response delay comes out if timing schedule adopted.

Thus in TF nodes, we need a "work-on-demand" method instead of channel listening periodically because the listening operations always consume too much extra energy. In order to shorten the response latency without sacrificing the energy efficiency, sensor node architecture with an independent secondary passive channel for "wakeup" has been proposed. The independent wakeup channel recovers the energy from the RF signal of the BS, and then arbitrates whether to start work, eliminating ineffective energy consumption.

III. Proposed Architecture

In the proposed architecture, a hybrid of active/passive RF is introduced. The benefits of "ultra-low-power" and "work-on-demand" are integrated smoothly by means of the secondary channel. Utilizing the passive RF which does NOT need to consume energy from local battery, the sensor nodes can "listen" passively in power-off mode of idle state with a much shorter response time, consuming almost zero idle power compared with traditional low-power ones.

1. System architecture

Fig.3 shows the architecture of the entire SoC. The SoC consists of 5 blocks: Power manager (PM), passive RF, active RF, digital core (including MCU, bootloader, memories) and sensor interfaces.

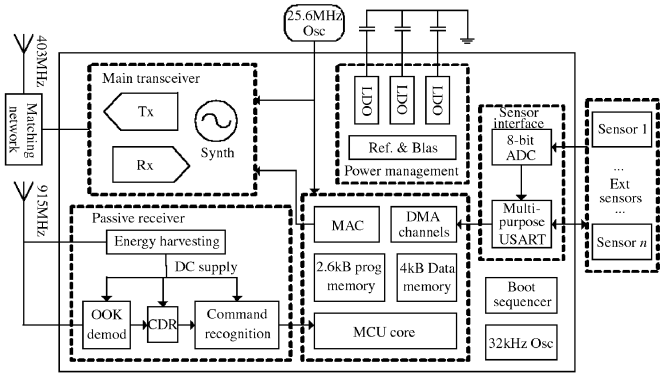


Fig. 3. Proposed system architecture of sensor nodes

In the SoC, the ULP MCU provides the functions of controlling and signal processing. The PM unit contains 3 programmable regulators (LDO's) which convert the battery voltage into specified voltages (0.9V, 1.8V, *etc*). An 8-bit 125ksps ADC with the successive approximation structure[7] is integrated. The 403MHz main transceiver with 200kbps TX and 64kbps RX is implemented to accomplish the burst data communication. Interfaces to other commercial transceiver parts are also provided to support WBSN's in various frequency

bands, and comply with different regulations.

The separate passive receiver based on energy-harvesting gives the SoC the unique capability of passive work-on-demand, which will be explained later. The entire SoC is highly integrated, and requires only a few external components to build a sensor node. Additionally, the SoC is powered by a 3V battery supply.

2. Dual-band concepts

Dual-band channels and RFs are utilized in the proposed architecture, avoiding the drawback of bulky and power hungry to implement system in Bluetooth and IEEE 802.11 for WBSN applications[8]. Though many researches are focused on the IEEE 802.15.4 (Zigbee), the optimizations are limited to the primary channel only[9−11].

The primary channel for data link is similar to most nonbeacon-enabled data transfer models, adopting half-duplex contention-based protocols. The up-link is for body information data transmission and the down-link is for configurations.

An independent secondary channel is utilized for listening to BS calling. The behavior of the secondary channel can be considered "passive", which means the sensor nodes do not need to afford energy consumption for the listening operation.

When in idle state, sensor nodes can be awaken by two events: local sleep time-out or BS event calls in. A timer is utilized to generate time-out. The control procedure is:

(1) MF nodes periodically collect and send data to BS;

(2) BS stores and analyzes the incoming data;

(3) If abnormal, BS transmit "emergency" beacon frame through the secondary channel;

(4) Only the node with correct ID wakes up immediately, even though all nodes may receive the beacon.

(5) Data communication link is established via the primary channel, which can also confirm the beacon operation in secondary channel.

Network response delay is a crucial aspect in the medical WBSN. Alternatively, if the sensor nodes turn most modules off in a low duty-cycle to meet the ULP requirement, they will probably miss emergency calls when in idle state.

The total consumed energy consists of both effective and non-effective parts: $E_{total} = E_{eff} + E_{noeff}$, and the energy efficiency is $C_{eff} = E_{eff}/E_{total}$. Note f_{arq} for re-transmission rate, E_{no-lis} for energy in idle state (mainly leakage), then

$$C_{eff} = E_{eff}/E_{total} \approx 1 - (Kf_{arq} + E_{no-lis})/E_{total}$$

IV. Implementation

The modules of grey blocks in Fig.3 are implemented in the SoC. The circuit of PM, transceiver, passive RF and digital core are elaborated to satisfy system requirements.

1. Power management

The PM module consists of a 20kHz oscillator, a timer for wake-up, a bootstrap sequencer, a bandgap bias and 3 Low drop-out regulators (LDOs).

The wake-up timer can count up to a maximum value of 420 seconds, which is sufficient for sleep state.

The bootstrap sequencer determines the key status of the system. Once sensor node is activated, the sequencer enables the output control signals in order: turns on bandgap → LDOs → enables clock → generates reset for digital core.

The sensor nodes have multiple low-power idle modes. When a sensor node is in work mode, all the modules are turned on to obtain adequate performance. In the idle mode the active RF module, transducer, regulators and oscillators are turned off to save energy, as listed in Table 1.

Table 1. Power modes in idle state

	Description	Wake up method
Standby	Timer & LDO on	Emergency call, or timer
Sleep	Timer on	Timer only
Power off	All modules off	Emergency call through Passive RF

The PM is powered directly by the battery, and there is only leakage current if PM turns all other modules off.

Level shifters with enabled buffer are inserted to convert the signal to correct voltage and connect the output signal to a stable voltage level when the input is floating, avoiding leakage current between the active / passive interfaces.

2. Passive RF

A passive RF receiver is implemented to detect the emergency beacon frame. The passive RF recovers energy from the carriers (in a different frequency from that of active RF) and then uses the energy to parse the commands. It is compatible with the protocol NCITS_256_1999[12], a widely adopted protocol in RFID. The protocol here is used for energy transmission together with the beacon frames.

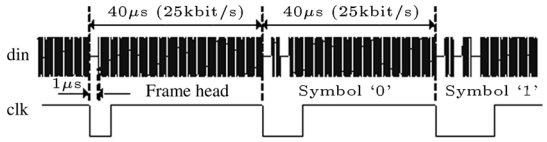


Fig. 4. Waveforms of bit definition in passive RF

The communication protocol in the secondary channel utilizes On-off keying (OOK) modulation. The bit definition in physical layer is shown in Fig.4. Bit '0' is represented by two consecutive negative pulses, and '1' is represented by three. The pulse width is 1μs nominally. In addition, one pulse is used to define the start and the end of a frame.

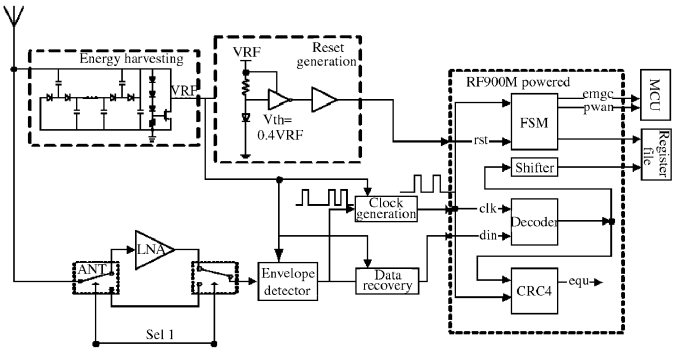


Fig. 5. Passive receiver based on energy harvesting

Fig.5 shows how the passive link-listening function is implemented in this SoC. A 25kbps OOK receiver including the

envelope detector, clock generation and data recovery is designed to work at 915MHz ISM band. The OOK receiver is powered by a DC voltage provided by an integrated energy harvesting block[13]. Note that in WBSN applications, the portable BS is usually powered by relatively larger batteries than sensor nodes. Thus with this SoC, when the sensor node works in the link-listening mode, only the energy harvesting circuitry and the OOK receiver are watching for the RF signal from the BS. The link-listening is continuous, and the SoC can achieve work-on-demand. A battery-powered LNA is optional to improve sensitivity of the OOK receiver. When the LNA is switched off, the OOK receiver does not consume any energy from the battery. The energy harvesting block can output a 1.2V supply with RF input down to −14dBm, and the OOK receiver consumes <2.7μA generally, and <20μA when the LNA is on.

The impedance of the antenna port is about (18-j10)Ω according to the measurement result from network analyzer. An L-shape matching network is added to match the 50Ω coaxial cable.

3. Transceiver

In typical WBSN applications, the data link speed is unequal in two directions. To optimize system power and simplify circuitry, the SoC has a 200kbps transmitter for the up-link and a 64kbps receiver for the down-link. Fig.6 shows the architecture of the 403MHz main transceiver.

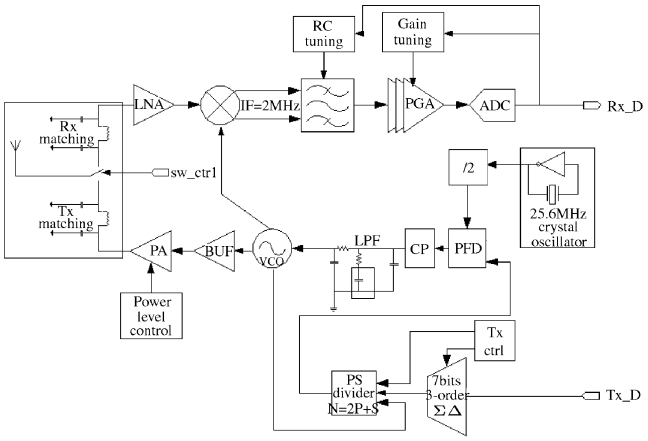


Fig. 6. 403MHz band Transceiver for data link

The low-IF architecture is a more attractive choice than zero-IF, since it holds the potential for an area-efficient monolithic integration of the transceiver combined with low power consumption and high performance[14]. Considering the receiver's factors such as 1/f noise, LO phase noise, power consumption, chip area and selectivity requirements, the IF-frequency of 2MHz was selected. A 6th order Chebyshev bandpass filter with a bandwidth of 1MHz was implemented for IF signal filtering.

A flexible and agile frequency synthesizer supporting narrow channel spacing and a high spectral purity is needed for the network. These requirements can be met with a fractional-N synthesizer[15].

(1) Its high reference frequency helps to avoid stray power in the adjacent channels. Low close-in phase noise is also important to maximize adjacent channel rejection.

(2) The wide loop bandwidth synthesizer allows fast settling, short startup and RX/TX turnaround time.

(3) The closed-loop transmitter modulation scheme is power-efficient and offers a superior quality.

(4) The fine frequency resolution with the fractional-N synthesizer relaxes the accuracy requirements of crystal frequency, facilitating the integration of an AFC loop.

The transceiver contains a ΣΔ PLL as the frequency synthesizer with a center frequency at 403MHz nominally. The up-link data is directly modulated into the PLL loop by alternating the frequency divider ratio[16]. The PLL consumes 2.5mA current from 1.8V supply with 200kbps data modulation. The PA following the PLL-based modulator can output up to −5dBm power with 0.61mA current consumption from 1.8V supply, which indicates a power efficiency of 29%. An OOK receiver with a raw BER of 10^{-3} and sensitivity of −85dBm has been implemented. After utilizing Reed-Solomon (31, 25) coding scheme and Automatic repeat-request (ARQ), the improved BER can reach 10^{-10}. The receiver provides a receiving speed from 20kbps to 64kbps, and it consumes 1.74mA current from 1.8V power supply maximally.

4. Digital core & sensor i/f

Fig.7 shows the architecture of the MCU. It contains a Wireless field-programming arbiter (WFPA), DMA controller, MAC, multi-purpose peripheral i/f, debug i/f and 6.6kB on-chip memory. With the WFPA, the sensor node can be reprogrammed remotely as needed, which gives the WBSN great convenience and flexibility.

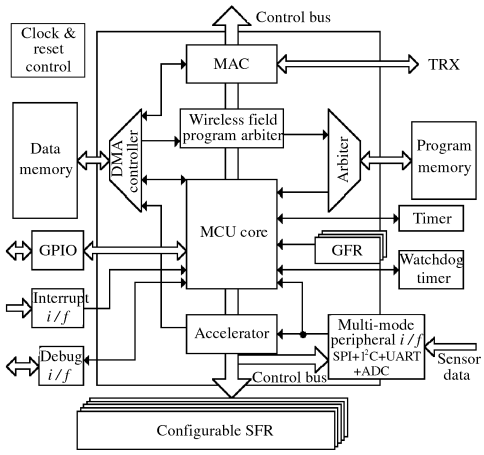


Fig. 7. Digital core functional blocks

The high-efficiency DMA controller helps to improve the system energy efficiency, especially for the situations of mass data transferring and processing.

DMA controller accomplishes mass data accessing as:

– Tx data path for data communication, from data memory to RF MAC.

– Rx data path for command communication, from RF MAC to data memory.

– WFPA data path, from data memory to instruction memory.

Additionally, hardware MAC integrates channel encoding/decoding, scramble, Clock data recovery (CDR), and

frame control. Moreover, the multi-purpose peripheral interface supports Universal asynchronous/synchronous receiver & transmitter (USART), such as SPI, I^2C, RS-232.

V. System Verification and Measured Results

The proposed WBSN sensor node verification has been validated in both FPGA and ASIC. An ARM7 board is utilized for the BS implementation.

In the FPGA verification, the digital core and PM are implemented in a Xilinx Virtex-4 test board. The peripheral active RF and the transducer for verification are proved to have correct behavior. Data received at the BS end are proved consistent with that collected from the sensor end.

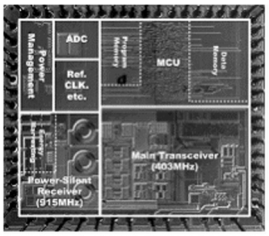
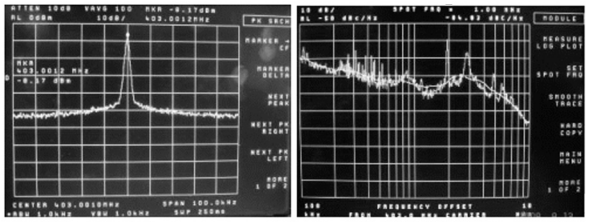


Fig. 8. Micrograph of the SoC

Fig.8 shows the micrograph of the SoC implemented in a 0.18μm RFCMOS technology. The entire chip occupies a die area of 5.9mm^2, including the core circuitry and the pad frame. The digital core and the power manager take a scale of 51.2k equivalent gate count excluding memories. When powered by 0.9V power supply and clocked by a 13MHz clock, it can provide a mean throughput of 2.5Mbps with only 165μW power consumption. Its power consumption can be even lowered to 42μW under operation-idle conditions.

The test result of RF module is shown in Fig.9, which is captured from spectrum analyzer. The Fig.9(a) shows the PA output when the transceiver is sending "1" and the PA power control is maximum. The output power is $-$8dBm with a frequency of 403MHz. The test result can reach $-$5dBm with off-chip separate matching networks. The Fig.9(b) shows the phase noise of the VCO when only TX module is working and RX module is powered off. The phase noise is $-$75dBc@100kHz, which is comparable to the simulation result $-$73dBc@100kHz.



(a) (b)

Fig. 9. Performance. (a) PA output spectrum; (b) TX phase noise

The overall performance of this SoC is summarized and compared to the results from Ref.[2] in Table 2. Though implemented in a more aged technology, the MCU in this work consumes much less power. The main transceiver in this work is comparable to the work in Ref.[2]. In the continuous link-listening mode, the unique passive receiver in this work makes the sensor node consume almost zero power, while a sensor node using SoC in Ref.[2] will consume at least 181J energy per day.

Table 2. Measured results

SoC		This work	Ref.[2]
Technology		0.18μm CMOS	0.13μm CMOS
Controller	Power supply	0.9V	1V
	Power consumption	165μW@13MHz*	500μW@1MHz
Passive Receiver	Frequency band	915MHz	Not available
	Modulation type	OOK	
	Sensitivity	$-$14dBm	
	Data Rate	25kbps	
Main Transceiver	Frequency band	403MHz	868/915MHz
	modulation type	TX FSK, RX OOK	FSK
	TX data rate	200kbps	50kbps
	PA output power	$-$5dBm**	$-$7dBm
	TX Power consumption	5.58mW ***	2.635mW
	RX data rate	64kbps	50kbps
	RX sensitivity	$-$85dBm with 10^{-3} raw BER	$-$102dBm with 10^{-3} raw BER
	RX power consumption	3.13mW	2.09mW
Energy per day: cont-listening		0	181J

*tested in a typical flow with duty-cycle of 1:8.
**based on measured data and calculated by matched networks.
***includes 4.5mW for synthesizer.

Additional, when in power-off mode of idle state, The passive RF consumes only leakage current from the battery during idle state. So the quiescent power can be neglected compared with others when passively listening to the BS. However, due to the leakage current from level shifter between modules, little quiescent current still exists in the prototype SoC.

VI. Conclusion

This paper looks into the key issues in WBSN, discusses the application specific requirements, and implements an energy efficient SoC avoiding tradeoffs such as low-power and instant-response. Sensor node architecture with a hybrid of active/passive RFs has been proposed to satisfy the instant wakeup demand with no extra energy induced in. It is especially helpful for long-term idle and low duty cycle TF nodes in the medical WBSN. The prototype system has been verified in both FPGA and 0.18μm process silicon.

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