A two-dimensional threshold voltage analytical model for metal-gate/high-k/SiO_2/Si stacked MOSFETs*

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In this paper the influences of the metal-gate and high-k/SiO_2/Si stacked structure on the metal–oxide–semiconductor field-effect transistor (MOSFET) are investigated. The flat-band voltage is revised by considering the influences of stacked structure and metal–semiconductor work function fluctuation. The two-dimensional Poisson's equation of potential distribution is presented. A threshold voltage analytical model for metal-gate/high-k/SiO_2/Si stacked MOSFETs is developed by solving these Poisson's equations using the boundary conditions. The model is verified by a two-dimensional device simulator, which provides the basic design guidance for metal-gate/high-k/SiO_2/Si stacked MOSFETs.

Keywords: metal-gate, high-k, work function, flat-band voltage, threshold voltage, metal–oxide–semiconductor field-effect transistor

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1. Introduction

With the size of a MOSFET scaling down to a sub-45 nm node, metal-gate/high-k technology has been recognized as a key process of transistor fabrication.[1] Metal and high-k dielectrics have replaced poly-Si and SiO_2 as the gate materials. Compared with the metal–oxide–semiconductor field-effect transistor (MOSFE) fabricated by poly-gate/SiO_2 technology, the high-k MOSFET has a small gate leakage current with an increased physical thickness of the gate dielectric.[2] The metal-gate materials do not react with high-k materials, and the sheet resistance is reduced. There is no gate depletion effect in the poly-gate material.[3] The metal-gate/high-k technology has become a promising candidate for the next generation MOSFETs. In order to improve the electrical properties of the metal-gate/high-k/Si stacked MOSFETs, it is necessary to introduce a thin interlayer of SiO_2 between the high-k dielectric and silicon.[4]

The threshold voltage of a MOSFET with a single high-k gate dielectric layer has been studied widely.[5−7] However, the threshold behaviour of the metal-gate/high-k/SiO_2/Si stacked MOSFET is rarely involved. The metal-gate and high-k/SiO_2 stacked structure can cause a new threshold voltage shift. The most direct expression of this threshold voltage fluctuation is the influence of charges at the high-k/SiO_2/Si interface and the metal work function fluctuation on the flat-band voltage. In this paper, considering the effect of the metal-gate/high-k/thin-oxide stacked structure on the flat-band voltage, a model of channel potential is obtained by solving the two-dimensional (2D) Poisson's equation, and the threshold voltage analytical model of a metal-gate/high-k/SiO_2/Si stacked MOSFET is developed. The analytical model is verified by using the 2D device simulator ISE-TCAD.

The rest of this paper is organized as follows. In Section 2 the effect of the stacked metal-gate/high-k/SiO_2/Si structure on the MOSFET is studied. In Section 3 the threshold voltage model of the metal-gate/high-k/SiO_2/Si stacked MOSFET is derived. In Section 4 the results of the threshold voltage model obtained in Section 3 are discussed. Finally, the conclusion is presented in Section 5.

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2. A metal-gate/high-k/ultrathin-SiO_2/Si stacked MOSFET

The schematic structure of a metal-gate/high-k/SiO_2/Si stacked n-channel metal–oxide–semiconductor field-effect transistor (nMOSFET) and the coordinates used in the solving process are shown in Fig. 1.

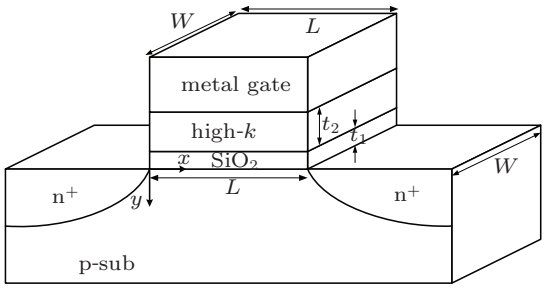

Fig. 1. Schematic structure of a metal-gate/high-k/SiO2/Si stacked nMOSFET.

A thin oxide layer, high-k dielectric material and metal gate are deposited on the substrate, sequentially. A three-layer sandwich structure is formed. The W and L are gate/channel width and length, respectively. The t_1 and t_2 are the physical thickness values of the oxide and high-k dielectric layer, respectively. The x axis is in the lateral channel direction and y axis is in the direction perpendicular to the channel.

2.1. Fluctuation of the metal-gate work function

The metal work function is defined as the minimum energy required for removing an electron from the Fermi level of a metal material to the vacuum level and making it a free electron. When the metal becomes the primary gate material in advanced CMOS technology, there is a new source of random variation due to the dependence of the work function on the orientation of the metal grain.[8] It has also become another factor which causes threshold voltage fluctuation.

From Fig. 1 we can see that the gate area is $W \times L$ and it contains many metal grains for a given material. The work function of each grain is a function of its orientation, which is not controllable during the growth period. Hence, the orientation of each grain is determined randomly.[9] It is known that metal grains usually grow up to a few nanometers in size under temperatures normally used in integrated circuit fabrication. Since the gate dimensions are in the order of a few tens of nanometers, it is expected that the gate contains a small number of grains. So the metal gate work function should be modeled as a probabilistic distribution rather than a deterministic value.[10] Table 1[11] shows the physical properties of some metal nitrides of the metal gate. Where titanium nitride (TiN) and tantalum nitride (TaN) are used for n-channel MOS (NMOS) devices, tungsten nitride (WN), and molybdenum nitride (MoN) are used for p-channel MOS (PMOS) devices.

Table 1. Physical properties of different metal nitrides as metal gates.[11]

Materials	Orientation	Probability	Work function/eV	Grain size/nm
TiN	⟨100⟩	60%	4.6	4.3
	⟨111⟩	40%	4.4	
TaN	⟨100⟩	50%	4.0	7
	⟨200⟩	30%	4.15	
	⟨220⟩	20%	4.8	
WN	⟨111⟩	65%	4.5	10
	⟨200⟩	15%	4.6	
	⟨220⟩	15%	5.3	
	⟨311⟩	5%	4.2	
MoN	⟨110⟩	60%	5.0	17
	⟨112⟩	40%	4.4	

According to the aforementioned results, we could conclude that the work function induced threshold voltage fluctuation is affected by the gate area, grain size, and the gate material. Yu *et al.*[1] proposed an analytic formula to describe the effect of work function fluctuation on threshold voltage fluctuation,

$$\Delta V_{\rm th} = A_{\rm VT}\sqrt{\frac{G}{A}}, \tag{1}$$

where G and A ($A = W \times L$) are the grain size and the gate area; $A_{\rm VT}$ is a fitting coefficient depending on the metal materials, the unit of $A_{\rm VT}$ is mV; the values of $A_{\rm VT}$ corresponding to TiN, TaN, WN, and MoN are 90, 283, 272, and 271, respectively. The fluctuation of the threshold voltage induced by metal work function fluctuation can be obtained by Eq. (1) when the gate area is small or the grain size is big. Based on Eq. (1), if the number of grains is big enough, the influence of the metal work function fluctuation on the threshold voltage can be ignored. According to the central limit theorem, the distribution of the metal work function is of approximately Gaussian distribution for the large number of grains ($\sim$ 10–100).[12] The metal work function can be modelled as a deterministic value as follows:

$$\Phi_{\rm M} = \sum_{i=1}^{N} \Phi_i P_i, \tag{2}$$

where Φ_i and P_i are used to identify the work function values of grains with different orientations and their corresponding probabilities.

Figure 2 shows the energy band diagram of a metal-gate/high-k/SiO_2/Si stacked structure under a thermal equilibrium. The values of $\chi_{\rm h}$, χ, and $\chi_{\rm ox}$ are the electron affinity of high-k dielectric, Si substrate, and oxide, respectively; V_i is the electric potential difference across the gate dielectric at zero gate voltage. The revised metal work function and electron affinity of the Si substrate are presented as follows:

$$\Phi'_{\rm M} = \Phi_{\rm M} - \chi_{\rm h}, \tag{3}$$

$$\chi' = \chi - \chi_{\rm ox}. \tag{4}$$

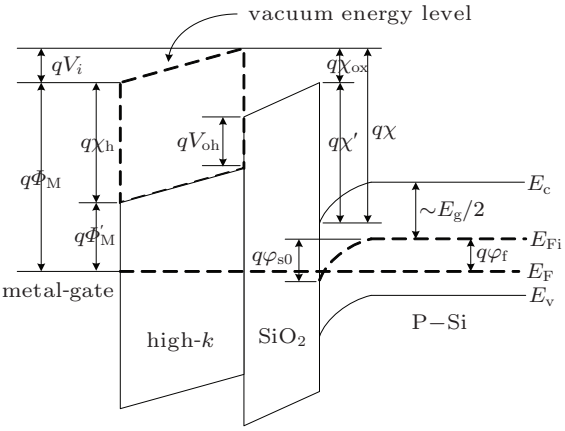

Fig. 2. Energy band diagram of the metal-gate/high-k/SiO2/Si stacked structure under a thermal equilibrium.

As shown in the figure, the sums of the Fermi energy level on both sides of the oxide are equal, i.e.,

$$q\Phi'_{\rm M} + qV_i + qV_{\rm oh} = q\chi' + \frac{E_{\rm g}}{2} - q\varphi_{\rm s0} + q\varphi_{\rm g}. \tag{5}$$

Equation (5) can be written as

$$V_i + \varphi_{\rm s0} = -\left[\Phi'_{\rm M} - \left(\chi' - V_{\rm oh} + \frac{E_{\rm g}}{2q} + \varphi_{\rm g}\right)\right], \tag{6}$$

where $V_{\rm oh} = \chi_{\rm h} - \chi_{\rm ox}$, and the work function difference between the metal and the semiconductor is defined as

$$\Phi_{\rm MS} = \Phi'_{\rm M} - \left(\chi' - V_{\rm oh} + \frac{E_{\rm g}}{2q} + \varphi_{\rm g}\right), \tag{7}$$

with

$$\varphi_{\rm g} = \frac{kT}{q}\ln\frac{N_{\rm A}}{n_{\rm i}}$$

being the Fermi potential, $E_{\rm g}$ the silicon band gap, and $n_{\rm i}$ the intrinsic carrier concentration.

2.2. Effect of a high-k/SiO_2/Si stacked structure

For a practical MOS structure, there are a certain quantity of fixed charges in the gate dielectric. The energy band is bent in the semiconductor. To counteract the bending, the applied gate voltage is defined as the flat-band voltage $V_{\rm fb}$,

$$V_{\rm fb} = \Phi_{\rm MS} - \frac{Q_{\rm ox}}{C_{\rm ox}}, \tag{8}$$

where $Q_{\rm ox}$ is the charge quantity (cm^{-2}) in the gate insulator layer, $C_{\rm ox}$ is the gate oxide capacitance per unit area. For a high-k/SiO_2/Si stacked structure, $Q_{\rm ox}$ is composed of four components, SiO_2/high-k dielectric bulk charges and charges at the SiO_2/Si and high-k/SiO_2 interface. Based on Ref. [13], the four components can be simplified. The SiO_2 and high-k bulk charges can be neglected since these bulk charge contributions are much smaller than that of the interface charges. So the flat-band voltage can be written as

$$V_{fb} = \Phi_{\rm MS} - \frac{Q_{\rm i}EOT_{\rm h}}{\varepsilon_{\rm ox}} - \frac{Q_{\rm g}EOT}{\varepsilon_{\rm ox}}, \tag{9}$$

where $Q_{\rm i}$ is the fixed charge at the high-k/thin-oxide interface, $EOT_{\rm h}$ and EOT are the equivalent oxide thickness values of the high-k layer and the total given gate stacks, respectively, $\varepsilon_{\rm ox}$ is the dielectric permittivity of the SiO_2, and $Q_{\rm f}$ is the effective fixed charge density at the oxide/Si substrate interface. All these components can be calculated by the capacitance-based method.[14–16]

However, there is a negative flat band shift when the equivalent oxide thickness is reduced to 2 nm.[17] When the oxygen diffuses through the gate dielectric, O exits in O^{2-} species and diffuses via an exchange with the lattice oxygen in the high-k layer.[18] Some O^{2-} form metal–O–Si bonds at the high-k/SiO_2 interface, and the others are converted into Si=O dipoles at the SiO_2/Si interface. Si atoms have partial positive charges and O atoms are partially negatively charged. These dipoles produce the electric field as shown in Fig. 3, which causes a negative $V_{\rm fb}$ shift. If the thickness of the SiO_2 layer is larger than the O^{2-} diffusion length, fewer dipoles are converted at the SiO_2/Si interface and thus produce a smaller electric field. Hence, a $V_{\rm fb}$ shift shows that it is closely related to the thickness of the SiO_2 layer. The $V_{\rm fb}$ shift can be calculated as follows:[19]

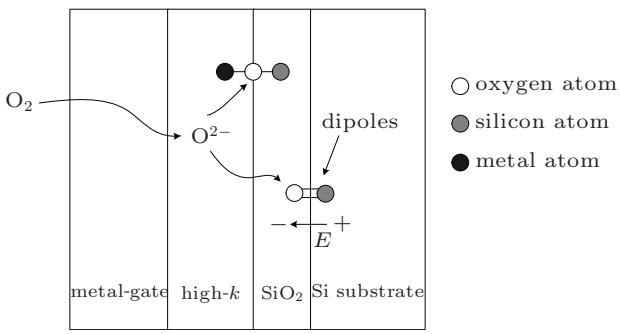

Fig. 3. Diffusion of O into SiO_2 layer from the high-k layer, forming dipoles with Si.

$$\Delta V_{\rm fb} = \alpha \exp\left(\frac{-t_1^2}{\beta}\right), \tag{10}$$

where α and β are fitting parameters related to process temperature, the values of α and β are 700 and 25, respectively, and t_1 is the thickness of the interface oxide layer. When t_1 decreases to a certain value, $\Delta V_{\rm fb}$ begins to increase rapidly. Considering the effect of dipoles, the flat-band voltage can be written as

$$V'_{\rm fb} = V_{\rm fb} + \Delta V_{\rm fb}. \tag{11}$$

3. Derivation of the threshold voltage model

Neglecting the mobile carriers in the channel depletion region, the 2D Poisson's equation in the channel region can be written as

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = \frac{qN_{\rm A}}{\varepsilon_{si}},$$
$$0 \le x \le L, \quad 0 \le y \le y_{\rm d}, \tag{12}$$

where $\phi(x,y)$ is the 2D potential distribution in the channel, $y_{\rm d} = \sqrt{4\varepsilon_{si}\varphi_{\rm g}/qN_{\rm A}}$ is the width of the depletion region in the substrate, $N_{\rm A}$ is the doping concentration of the substrate, and ε_{si} is the dielectric permittivity of the substrate. Using a two-order polynomial approximation, $\phi(x,y)$ can be written as

$$\varphi(x,y) = \varphi_0(x) + \varphi_1(x)y + \varphi_2(x)y^2. \tag{13}$$

To solve the parabolic function, the boundary conditions are shown as follows.

(i) At the SiO_2/Si interface ($y = 0$), the 2D surface potential distribution can be written as

$$\varphi(x,0) = \varphi_0(x). \tag{14}$$

(ii) The electric flux (displacement) at the SiO_2/Si interface ($y = 0$) is continuous, i.e.

$$\left.\frac{{\rm d}\varphi(x,y)}{{\rm d}y}\right|_{y=0} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{si}} \frac{\varphi(x,0) - V_{\rm gs} + V'_{\rm fb}}{EOT}, \tag{15}$$

where $EOT = t_1 + EOT_{\rm h} = t_1 + t_2\varepsilon_{\rm ox}/\varepsilon_{\rm h}$; $\varepsilon_{\rm ox}$ and $\varepsilon_{\rm h}$ are the dielectric permittivity of SiO_2 and the high-k dielectric, respectively; $V_{\rm gs}$ is the gate-to-source bias voltage; $V'_{\rm fb}$ is the revised flat-band voltage.

(iii) At the depletion edge ($y = y_{\rm d}$), the boundary conditions are shown as follows:

$$\begin{cases} \varphi(x, y_{\rm d}) = V_{\rm bs}, \\ \left.\dfrac{{\rm d}\varphi(x,y)}{{\rm d}y}\right|_{y=y_{\rm d}} = 0, \end{cases} \tag{16}$$

where $V_{\rm bs}$ is the substrate voltage, while the substrate is grounded, i.e., $V_{\rm bs} = 0$.

The values of the coefficients $\phi_i(x)$ (i = 0, 1, 2) in Eq. (13) can be determined using the boundary condition Eqs. (14)–(16). Substituting Eq. (13) into Eq. (12) and setting $y = 0$, the two-order differential equation about $\phi_0(x)$ can be obtained as

$$\frac{\partial^2 \varphi_0(x)}{\partial x^2} - P\varphi_0(x) = Q, \tag{17}$$

where

$$P = \frac{\varepsilon_{\rm ox}}{y_{\rm d}\varepsilon_{si}EOT}, \quad Q = \frac{qN_{\rm A}}{\varepsilon_{si}} - \frac{\varepsilon_{\rm ox}}{y_{\rm d}\varepsilon_{si}EOT}(V_{\rm gs} - V'_{\rm fb}).$$

The solution for Eq. (17) is a simple second-order non-homogenous differential equation with constant coefficients, and it can be written as

$$\varphi_0(x) = A\exp(\lambda x) + B\exp(-\lambda x) - D, \tag{18}$$

where $\lambda = \sqrt{P}$, $D = Q/P$, A and B are the coefficients that can be determined by the following boundary conditions:

i) the surface potential at the source end is

$$\varphi(0,0) = \varphi_0(0) = V_{\rm bi}, \tag{19}$$

ii) the surface potential at the drain end is

$$\varphi(L,0) = \varphi_0(L) = V_{\rm bi} + V_{\rm ds}, \tag{20}$$

where

$$V_{\rm bi} = \frac{kT}{q} \ln \frac{N_{\rm A} N_{\rm D}}{n_i^2}$$

is the built-in potential of the drain/source-substrate junction, with $N_{\rm D}$ being the doping concentration of the source/drain regions and $n_{\rm i}$ the intrinsic carrier concentration; $V_{\rm ds}$ is the drain-to-source bias voltage.

Based on Eq. (18), the minimum surface potential ($\phi_{0,\rm min}$) can be determined by $\mathrm{d}\varphi_0(x)/\mathrm{d}x = 0$. Setting $\varphi_{0,\rm min} = 2\varphi_{\rm g}(\varphi_{\rm g} = (kT/q)\ln(N_{\rm A}/n_i))$, the corresponding gate voltage $V_{\rm gs}$ is defined as the threshold voltage $V_{\rm th}$

$$V_{\rm th} = \frac{qN_{\rm A} y_{\rm d} EOT}{\varepsilon_{\rm ox}} + V'_{\rm fb} - \frac{-b + \sqrt{b^2 - 4ac}}{2a}, \tag{21}$$

where

$$\begin{aligned} a &= \sinh^2(\lambda L) - 2\cosh(\lambda L) + 2, \\ b &= [2 - 2\cosh(\lambda L)](2V_{\rm bi} + V_{\rm ds}) + 4\varphi_{\rm g}\sinh^2(\lambda L), \\ c &= [2 - 2\cosh(\lambda L)](V_{\rm bi}^2 + V_{\rm bi}V_{\rm ds}) \\ &\quad + 4\varphi_{\rm g}^2 \sinh^2(\lambda L) + V_{\rm ds}^2. \end{aligned}$$

4. Results and discussion

According to the aforementioned analysis, we can see that the revised flat-band voltage $V'_{\rm fb}$ is a key parameter of the threshold voltage. From Eq. (11), it can be found that the revised flat-band voltage is composed of two parts ($V_{\rm fb}$ and $\Delta V_{\rm fb}$). The former $V_{\rm fb}$ is caused mainly by the metal work function and charges in the gate insulator layers, and the latter $\Delta V_{\rm fb}$ is induced chiefly by dipoles at the SiO_2/Si interface.

Figure 4 shows the dependence of revised flat-band voltage $V'_{\rm fb}$ on the interface oxide thickness t_1. We keep the total equivalent oxide thickness EOT constant (=2 nm), and increase the interface oxide thickness t_1 from 0.1 nm to 1.9 nm (equivalent thickness of the high-k layer $EOT_{\rm h} = EOT - t_1$). It can be seen from the figure that the flat-band voltage shift $\Delta V_{\rm fb}$ decreases as t_1 increases, which is consistent with the result of Eq. (10). With the increase of t_1, the number of oxygen ions diffusing through the oxide decreases. Fewer dipoles are converted at the SiO_2/Si interface, and a smaller electric field is obtained. However, with the increase of t_1, $V_{\rm fb}$ increases according to Eq. (9). So the revised flat-band voltage $V'_{\rm fb}$ decreases at the beginning and then increases.

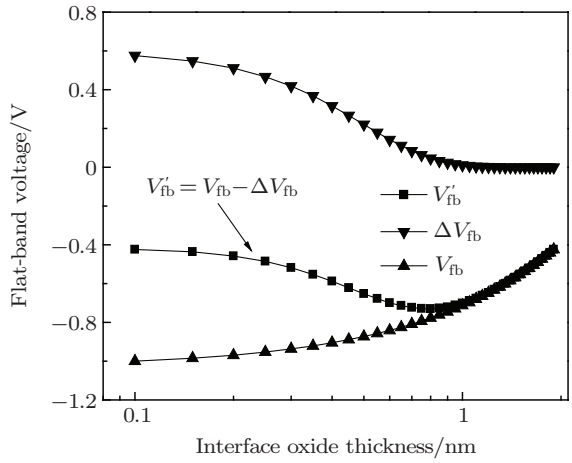

Fig. 4. Variations of the revised flat-band voltage $V'_{\rm fb}$ with an interface oxide thickness t_1. TiN and HfO_2 are used as the gate material and high-k material, respectively. $N_{\rm A} = 2\times10^{18}$ cm^{-3}, $N_{\rm D} = 1\times10^{20}$ cm^{-3}, $EOT = 2$ nm, $L = 45$ nm, $V_{\rm ds} = 1.0$ V.

Figure 5 shows the variations of the revised flat-band voltage $V'_{\rm fb}$ with the total equivalent gate oxide thickness EOT. The interface oxide thickness t_1 is kept constant (=0.5 nm). Based on Eq. (10), the flat-band voltage shift $\Delta V_{\rm fb}$ is the same. The increase of the total equivalent gate oxide thickness EOT means the increase of equivalent high-k thickness $EOT_{\rm h}$, and the $V_{\rm fb}$ decreases according to Eq. (9). So the revised flat-band voltage $V'_{\rm fb}$ decreases with the value of EOT increasing.

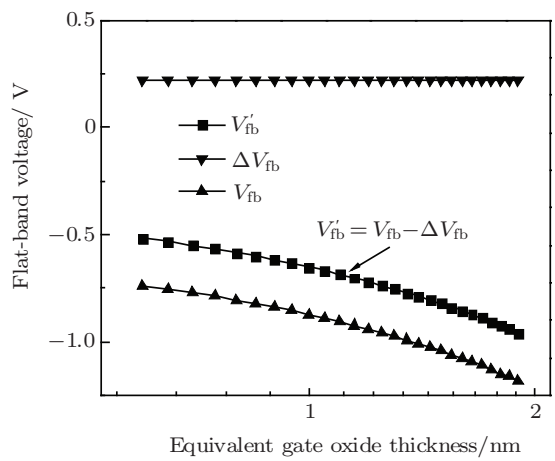

Fig. 5. Variations of revised flat-band voltage $V'_{\rm fb}$ with total equivalent gate oxide thickness EOT. TiN and HfO_2 are used as the gate material and high-k material, respectively. $N_{\rm A} = 2\times10^{18}$ cm^{-3}, $N_{\rm D} = 1\times10^{20}$ cm^{-3}, $t_1 = 0.5$ nm, $L = 45$ nm, $V_{\rm ds} = 1.0$ V.

In order to verify the proposed analytical threshold voltage model, an nMOSFET with a metal-

gate/high-k/SiO_2 stacked structure is used. The analytical results of the threshold voltage calculated from the model are compared with the numerical results obtained by the 2D device simulator ISE-TCAD. The relationship of the key device parameters and the threshold voltage is analysed.

Figure 6 shows the dependence of the threshold voltage $V_{\rm th}$ on the substrate doping concentration $N_{\rm A}$. For the same device structure, doping profile and geometrical dimensions are used in both analytical model and 2D numerical simulations. Good agreement is obtained between the prediction from the analytical model and the 2D numerical simulation results. For nMOSFETs with a constant source/drain region doping concentration $N_{\rm D}$, the threshold voltage $V_{\rm th}$ increases with the increase of substrate doping concentration $N_{\rm A}$. When the acceptor impurity concentration in the channel region increases, the thickness of the channel inversion layer decreases, and the source to drain current gradually decreases. A larger gate voltage is required to turn on the channel.

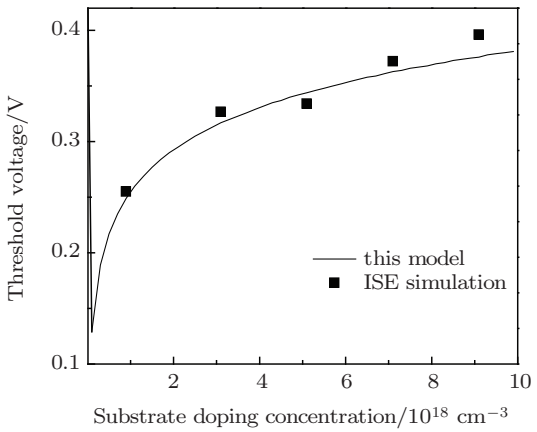

Fig. 6. (colour online) Variation of the threshold voltage $V_{\rm th}$ with substrate doping concentration $N_{\rm A}$. TiN and HfO_2 are used as the gate material and high-k material, respectively. $N_{\rm D} = 1 \times 10^{20}$ cm^{-3}, $EOT = 1$ nm, $EOT_{\rm h} = t_1 = 0.5$ nm, $L = 45$ nm, $V_{\rm ds} = 1.0$ V.

Figure 7 shows the dependence of the threshold voltage $V_{\rm th}$ on channel length L. For a given channel doping concentration, the threshold voltage $V_{\rm th}$ increases with the increase of channel length due to the reduction in influence of the source and drain junction depletion layers. In other words, with the channel length shrinking, the depletion layer widths of the source and drain region make an effective channel length decrease. The current from source to drain increases, which leads to a lower threshold voltage. It can be seen from the figure that the threshold voltage $V_{\rm th}$ increases with gate length L increasing. The results derived from the analytical model accord well with the ISE-TCAD simulation results.

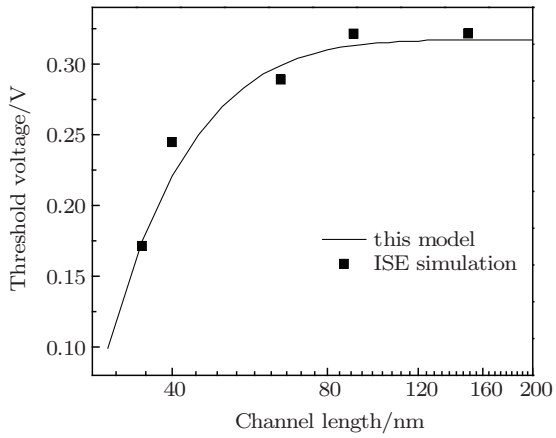

Fig. 7. Variation of the threshold voltage $V_{\rm th}$ with channel length L. TiN and HfO_2 are used as the gate material and high-k material, respectively. $N_{\rm A} = 2 \times 10^{18}$ cm^{-3}, $N_{\rm D} = 1 \times 10^{20}$ cm^{-3}, $EOT = 1$ nm, $EOT_{\rm h} = t_1 = 0.5$ nm, $V_{\rm ds} = 1.0$ V.

Figure 8 shows the dependence of the threshold voltage $V_{\rm th}$ on the drain voltage $V_{\rm ds}$. Similarly to the mechanism for the effect of channel length on the threshold voltage, the threshold voltage $V_{\rm th}$ decreases as the drain voltage $V_{\rm ds}$ increases. When the channel length and doping concentration are fixed, the width of the drain junction depletion layer increases with the drain-to-source bias voltage increasing. The effective channel length decreases, and a lower threshold voltage is obtained. So the threshold voltage decreases with increasing drain voltage. The results obtained from the model agree well with the ISE-TCAD simulation results.

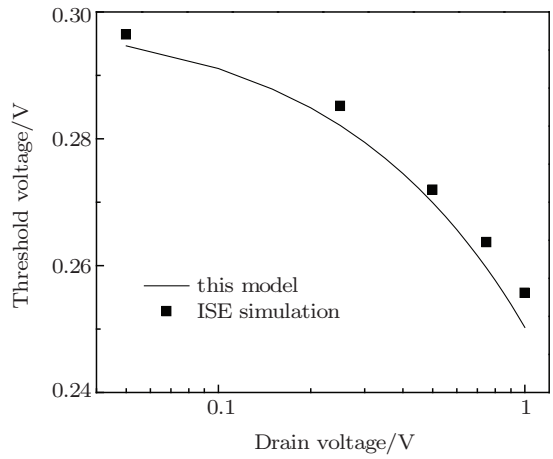

Fig. 8. Variation of the threshold voltage $V_{\rm th}$ with the drain-to-source bias voltage $V_{\rm ds}$. TiN and HfO_2 are used as the gate material and high-k material, respectively. $N_{\rm A} = 2 \times 10^{18}$ cm^{-3}, $N_{\rm D} = 1 \times 10^{20}$ cm^{-3}, $EOT = 1$ nm, $EOT_{\rm h} = t_1 = 0.5$ nm, $L = 45$ nm.

5. Conclusion

In this paper, the metal-gate/high-k/SiO_2/Si stacked structure is presented. The influence of metal-gate and high-k stacks on the flat-band voltage is investigated. The revised metal–semiconductor work function and revised flat-band voltage are obtained. The two-dimensional potential distribution Poisson's equation is developed and also solved using the boundary conditions. A threshold voltage analytical model for a metal-gate/high-k/SiO_2/Si stacked MOSFET is presented, which is consistent with the simulated results.

References

[1] Yu C H, Han M H, Cheng H W, Su Z C, Li Y M and Watanabe H 2010 *Proceedings of the 2010 International Conference on SISPAD* September 6–8, 2010, Bologna, Italy, p. 153

[2] Li J, Liu H X, Li B, Cao L and Yuan B 2010 *Acta Phys. Sin.* **59** 8131 (in Chinese)

[3] Luan S Z, Liu H X, Jia R X, Cai N Q and Wang J 2008 *Acta Phys. Sin.* **57** 4476 (in Chinese)

[4] Robertson J 2006 *Rep. Prog. Phys.* **69** 327

[5] Liu X Y, Kang J F, Sun L, Han R Q and Wang Y Y 2002 *IEEE Electron Dev. Lett.* **23** 270

[6] Ji F, Xu J P and Lai P T 2007 *Chin. Phys.* **16** 1757

[7] Xie Q, Xu J, Ren T L and Taur Y 2010 *Semicond. Sci. Technol.* **25** 035012

[8] Chen H W and Li Y M 2010 *14th International Workshop on Computational Electronics* October 26–29, 2010, Pisa, Italy, p. 1

[9] Frye A, Galyon G T and Palmer L 2007 *IEEE Trans. Electron. Packag. Manf.* **30** 2

[10] Dadgour H F, Endo K, De V K and Banerjee K 2010 *IEEE Trans. Electron Dev.* **57** 2504

[11] Rasouli S H, Endo K and Banerjee K 2010 *IEEE/ACM International Conference on Computer-Aided Design* November 7–11, 2010, San Jose, Ca, USA p. 714

[12] Dadgour H F, Endo K, De V K and Banerjee K 2008 *IEEE International Electron Devices Meeting* December 15–17, 2008, San Francisco, USA, p. 1

[13] Kerber A, Cartier E, Pantisano L, Degraeve R, Kauerauf T, Kim Y, Hou A, Groeseneken G, Maes H E and Schwalke U 2003 *IEEE Electron Dev. Lett.* **24** 87

[14] Jha R, Gurganos J, Kim Y H, Choi R, Lee J and Misra V 2004 *IEEE Electron Dev. Lett.* **25** 420

[15] Wen H C, Choi R, Brown G A, Boscke T, Matthews K, Harris H R, Choi K, Alshareef H N, Luan H F, Majhi P, Kwong D L and Lee B H 2006 *IEEE Electron Dev. Lett.* **27** 598

[16] Choi K, Wen H C, Bersuker G, Harris R and Lee B H 2008 *Appl. Phys. Lett.* **93** 133506

[17] Lee B H, Oh J, Tseng H H, Jammy R and Huff H 2006 *Mater. Tody* **9** 32

[18] Foster A S, Shluger A L and Nieminen R M 2002 *Phys. Rev. Lett.* **89** 225901

[19] Zheng X H, Huang A P, Xiao Z S, Yang Z C, Wang M, Zhang X W, Wang W W and Chu P K 2010 *Appl. Phys. Lett.* **97** 132908