A New Carry-free Adder Model for Ternary Optical Computer

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***Abstract*—Based on parallelism of MSD addition, a new carry-free adder model for optical computer is proposed. Using MSD number system and four kinds of logic transforms, the model is built with input part and three optical calculators. With the model, addition is implemented with only logic operations without any carry. This can greatly improve the efficiency of addition operation. To guarantee the feasibility of the implementation of the model, the alignment issue between the data bits of operands on different optical calculators is discussed. And the method to solve the problem that the input state of light is dark while the output state is bright in the process of logic transform is put foward. The analysis results show that the model is correct and can much improve the efficiency of the adder compared with the traditional adder model.**

Keywords- optical computer; MSD algorithm; adder model; alignment of operand; redundancy

I. INTRODUCTION

Modefied signed-digit (MSD) addition was proposed in 1961 by Avizienis for the first time. It is a kind of parallel algorithm based on MSD digital system[1,2] which presents information in redundant digital form. The characteristic of MSD addition is that it is a carry-free method which means it can avoid carry propagation between the adjacent data bits in the process of addition operation. This is a big advantage over traditional addition methods and implementation. It can infer that in MSD addition, what affect the efficiency of addition operation most is not the number of bits of operands as other addition methods do but the MSD addition's logical steps.

Space parallelism is one of the absorbing characteristics of optical operation, which guarantees that addition operation in optical computer can use MSD schema to exploit the advantage of optical computing. While the development of ternary optical computer (TOC) has made great achievement, the applications of it is still confined to logical operations for some reasons, among which lack of adder is one of the main hinders. Of course, following the steps of MSD transforms, addition can also be implemented on the ternary optical computer. However, it at least needs to transform three times in sequence to execute a addition operation. What is more, these three transforms are complete in serial. That is, the inputs of the latter transforms are the feedback of the results of the former operations. This makes the addition operation be much inefficiency.

As addition operation is the basis of numerical computing applications, it is very necessary to develop an efficient adder for ternary optical computer to proceed additional operation. This paper is try to present an efficient adder model that can be used in TOC to promote its use not in logical operations but also arithmetic areas.

II. BASIS OF THE RESEARCH

Before discussing the new adder model proposed in this paper, it's necessary to give a brief introduction of two points both of which are the basis of the study. One point that need to be mentioned is ternary optical computer's operational unit[3] and the other one is MSD additional algorithm[2].

A. TOC's Operational Unit

The conception of TOC[4] was proposed by Professor JinYi at Shanghai University firstly in 2000. Since then, the group led by Prof. Jin himself have set much effort on the study of Ternary Optical Computer and much achievement[5,6,7,8] has been made. Among the numerous achivements, the successful development of the experiment system with thousands of bits is a big marvel. With the experiment system, all optical operations can be realized through reconfiguration[3] of the operational unit according to the truth table user provided. The structure of basic unit which is used to make up of logical operational unit is demonstrated in figure 1. Where Lcd array is used to proceed lights passing through and polaroid signed p1 and p2 is exploited to serve as selector of passing lights. The polarization of light passing through LCD is controlled by the control signal put on the LCD. That is, light might changes polarization after it passes through the LCD if only the control signal is suitable. There are two kinds of polaroid, one is horizontal type and the other vertical one. Horizontal Polaroid only allowes horizontal polarized lights pass through. For the same reason, vertical polaroid just enable vertical polarized lights pass through. According the theory of Decrease-Radix Design principle, a bit of operator for any kind logical operation can be implemented by several basic units presented in figure 1.

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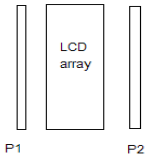

Figure 1. Structure of basic unit.

B. MSD Parallel Additional Algorithm

MSD is a kind of redudant digital number system[1,2]. Based this number system, MSD addition algorithm can implement parallel addition operation only with three carry-free logic operation. In this paper a new carry-free optical addition's model is presented based on MSD addition algorithm together with newly developed TOC.

Table 1 is the truth table of the four kinds of logical operation used in MSD addition which are operation T, W, T' and W'. Where -1 in table 1 represents vertical lights in the process of optical addition operation. 0 represents dark state and 1 horizontal light state respectively.

As more details of the discussion about MSD addition please refer literature [2] for reference.

TABLE I. FOUR KINDS OF TRUTH TABLE FOR MSD ADDITION

T a\b	-1	0	1	W a\b	-1	0	1	T' a\b	-1	0	1	W' a\b	-1	0	1
-1	-1	-1	0	-1	0	1	0	-1	-1	0	0	-1	0	-1	0
0	-1	0	1	0	1	0	-1	0	0	0	0	0	-1	0	1
1	0	1	1	1	0	-1	0	1	0	0	1	1	0	1	0

III. EASE MODEL OF ADDER FOR TOC

A. Carry-Free Adder's Model

The architecture of the adder model we proposed is demonstrated in figure 2. From the figure, it is not hard to figure out that the adder is physically consisted of four separate parts while logically in two parts. The left of the adder is the input part. It answers for light input and optical encoding. The right part of the adder is the addition operation. It consists of three group of sequentially arrayed logical operational units. The logical operational units of the adder is implemented with LCD, polaroid and light sensitive cell. The function of the encoding part is try to encode the natural light inputted to ternary output light. The encoded light will be used as the input of addition operators. The first logical operational units implement T operation and W operation at the same time, the second part proceeds T' and W' operations and the third realizes T operation. The function of additional embedded system is to create LCD's control signal and send them to LCD.

B. Determination of the Result of Logic Operation

According to theory of Decrease-Radix Design principle[3], one bit of operand needs a HH type operation unit and a VV type operation unit to complete T' operation. Signal H means horizontal type polaroid while V means vertical type polaroid. In HH type operation unit both p1 and p2 are horizontal polariods .

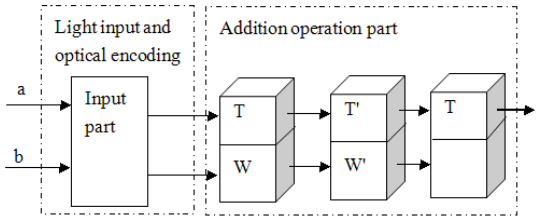

Figure 2. Adder's Model with Carrying Free Character.

From the output state of light sensitive cell which is expressed with 0 or 1, decoder can judge the result of logical operational units. Signal 0 and 1 mean dark state and bright state respectively. Based on the signal and the type of polaroid before crystal, the decoder can decode result of the light sensitive pixel. If output of one light sensitive spot is 1 and polaroid before the spot is V type, the result of the operational unit is vertical light. If the output of light sensitive spot is 1 and the polaroid before the spot is H type, the result of the spot is hoizontal light. And if the output of one light sensitive spot is 0, the result of the operational unit is no light.

The result of one bit operand for T' operation is determined by the results of one HH type operation unit and one VV unit. If the result of HH operational unit is horizontal light, one bit operand's result of T' operation is horizontal light. Else if the result of VV unit is vertical light, one bit operand's result of T' operation is vertical light. Otherwise this bit operand's result of T' operation is no light.

C. Adder's Working Process

Based on MSD additional algorithm and TOC, the working process for carry-free adder is as follows.

- Input operand and obtain the input light after it passes through the encoder. The input light can be expressed by a in the transform T and W of the truth table. In the process of addition, one of the most important factors is the control signal exerted on LCD. This signal is sent out from the embedded system. It is much related to the addend and the value of b in the truth table. With the direction of suitable signal, we can obtain the results of operation T and W.
- The input of the operation of T’ and W’ is the output light of operation T and W, they are expressed by a in the truth table. The control signal on LCD in the process of operation of T’ and W’ is much related to the value of b in the truth tatble. The second logic operation part is mainly used to implement the operation of T’ and W’.
- The input of the third logic part is the result of the second logic operation part. That is, the result of T’

is expressed with value a in the truth table. The control signal on the LCD of the third logic part is much related to the result of W' operation and the operator b in the truth table. The third logic operation part is to implement the operation of T.

- The result of the third part is sent to the embedded system and then returned to user as the final result of addition.

IV. Alignment Issue between the Data Bits of Operands on Different Optical Calculators

It is necessary to solve the problem of alignment between the data bits of operands on different optical calculators, because after T operation operant result of location i need to be located at i+1.

The alignment of hardware for T, T' and T operation on three part presents in figure 3. Line a* means that the operant a has been shifted left for two bit with two zeros complemented on the right. This indicates that the number on the place of a1 is right most number before the shift. Line T gives the rule how the number of the result will be arranged after the operation T on the first operation part. Line t' is the rule how the number of the result will be arranged after the operation T'. The bottom line T is the arrangement of the number of the result after the operation T executed on the third logic part.

a*	a2	a1	0	0
T	t3	t2	t1	0
T'	t'4	t'3	t'2	t'1
T	t4	t3	t2	t1

Figure 3. Hardware's Alignment.

It can see from figure 3 that a1 is the lowest bit of the addend of operation T. The control signal is determined by the lowest bit of addend b. T2 is the output of of the result of the addition of the lowest bit. The result of the first bit of operation T is placed at t2. With this rule, the alignment of bits will be implemented following the formula $t_i = T(x_{i-1}, y_{i-1})$. To the operation T', the input is t2, the result of the operation T. The control signal is created by the sencond bit of operation W. And it's result is symbol t'3, the third bit of operation T'. With this rule the alignment is implemented $t_i' = T'(t_{i-1}, w_{i-1})$. Operation T on the third logic operation part is something like that on the first logic part. Its input is symbol t'3, the control signal on LCD is determined by the third bit of operation W' and it's result is t3. This can implement the alignment of $t_i = T(t_i', w_i')$.

V. The Realization of One Bit Addition

A. Related issue

When observing the truth table of T and W' operation, it's not hard to find that there exists a case that input a is no light while output has light. In T operation's truth table, a and b correspond to T operation's input and LCD's control signal respectly. Result is 1 when a is 0 and b is 1 which means the input is no light but the result is horizontal polarized light.

It's impossible that result is bright while its input is dark according to the physical characteristics of lighting device. The TOC's traditional solution is try to change no light state input into states with light through logical conversions before sending to operational units. For in carry-free adder, result of operating unit is put into the next operating unit directly as input, there has no opportunity to do logical conversion. Traditional method is useless and new solution for this issue is needed to be researched.

B. Redundant light method

When analysing logical operations of MSD addition, we have two conclusions, one is that the above issue only present in operation T and W' and the other is only when the input a and b are both 0, the result is 0. So redundant light route method is considered to solve this issue.

Two models of W'1 and redundant W'2 work together to accomplish the function of W' operation. W' operations with a being non-zero in the truth table is implemented by W'1 model. In these operations, the input and control signal of W'1 is the result of W operation and determined by the result of T operation. The other operations in the truth table, that is, W' operation with a being 0 is implemented by W'2 redundant model. In these operations, the input and control signal of W'2 is the result of T operation and determined by the result of W operation. The principle of W' operation presents in figer 4 where module 1 and module 2 implement W operation separately on the same time and module 3 and module 4 implement T operation separately in synchronization. So the inputs of one-bit W' operation is the results of two separate W operations and two T operations. That is, one part input is the result of two W operations and the other input is the result of two T operations. In the real application, the result of W operation is to implment the operations with a being non-zero in the truth table while the result of T operation is to fulfill the operation with a being zero in the table. To implement W' operation, two logic operation units are needed, one is HV type unit and the other is VH type unit. The results of two T operations and W operations are the inputs of both HV and VH type units. The result of the operation of module 1 and module 2 in figure 4 serves as the input of module W'1 while the result of the operation of module 3 and module 4 serves as the input of the redundant module W'2. Both W'1 and W'2 are to implement W' operation.

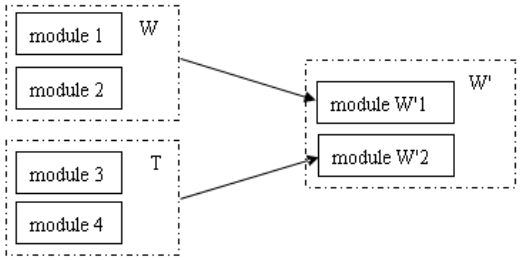

Figure 4. Physical structure of W' Operation.

To the T operation on the right most of figure 1, the inputs a and b are the results of T' operation and W' operation respectively. And it is implemented by T1 module and redundant module T2. Where T1 tries to implement the operations with a being non-zero in truth table while the result of T2 operation answers for the implementation of the operations with a being zero. In the process of operations, control signal in T1 and T2 is produced by the result of W' and T' operation respectively. The principle of T operation is as shown in figure 5 where module 1 and 2 in the upper dotted line box answer for T' operation while module 3 and 4 in the bottom dotted line box try to implement W' operation. The results of module 1 and 2 are the two inputs of module T1 and the results of module 3 and 4 are the two inputs of module T2. Both T1 and T2 are to implement T operation.

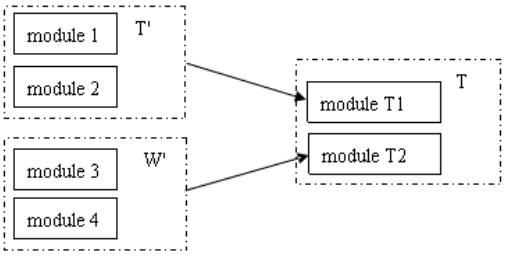

Figure 5. Physical Structure for T Operation.

In part one, a bit operand of T operation needs one VV and one HH logic operation units. A bit operand of W operation needs a VH and a HV logic operation units. In part two, a bit operant of T' operation needs a VV and a HH logic operation units. A bit operant of W' operation needs a VV and a HH logic operation units. As mentioned above, the case input is dark state while output is bright is impossible. This issue can be solved by redundancy of light path. Combine W' operation and redudant light path of T operation, the structure of one bit operand is as figure 6 shown.

VI. Analysis of the Model

To implement MSD addition, traditional method needs to reconfiguration the logic operation units and feedback the temp results in the transforms at least three times[9]. This makes the addition operation is very inefficient. Using the carry-free adder model proposed in this paper, in the process of addition no data feedback of the temp results is needed and only one reconfiguration of the logic operation units is needed. This means that the extra time in the process of addition in the proposed method is much less than that of the tradition method. That is, the new method is more efficient over the traditional method.

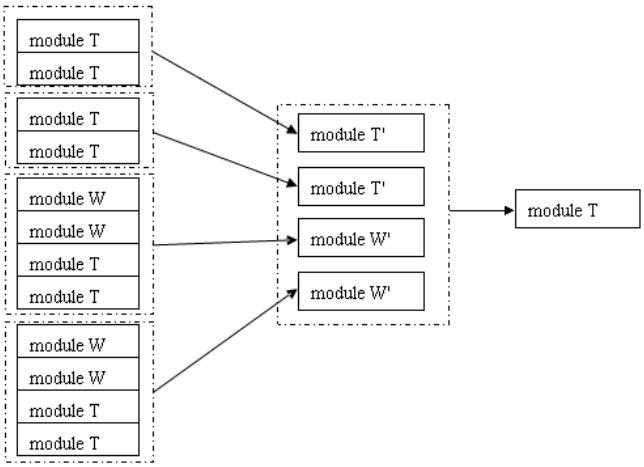

Figure 6. Physical Structure for Addition's One Bit Operand.

Table 2 presents a brief comparison between the implementation of the proposed optical adder and that of the traditional method. From the table, it is not easy to find that all the operations such as result image capture, decoding, data feedback, reconfiguration of logic operation units and so on need to be executed three times in traditional method, while only need to be executed once at most in the new proposed method. It can infer that the efficiency of the adder following the proposed method will be at least twice that of adder following the traditional method.

TABLE 2 Comparison of the Proposed Method with Traditional Method

Items \ Method	Traditional method	Carry-free adder
Result image capture times	3	1
Decoding times	3	1
Feedback times	3	0
reconfiguration times of logic operation units	3	1

VII. Conclusion

Carry-free adder's model is proposed in this paper. Based on MSD additional algorithm this model can process additional operation for the numbers with huge number of bits and it can fully exploit the parallel character of optical computer. Compared with traditional method it is more efficient for addition operation. For using the model implement addition, no decoding and feedback is needed. The analysis results show that this model is correct and is better than traditional method. The future work is to realize

the optical adder under the direction of model, so that the TOC can better be used in numerical computation area.

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