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A common-mode BIST technique for fully-differential sample-and-hold circuits

Jun Yuan[a)] **and Masayoshi Tachibana**[b)]

Electronic and Photonic System Engineering, Kochi University of Technology, Tosayamada-cho, Kochi, 782–8502, Japan

a) *138007b@gs.kochi-tech.ac.jp*

b) *tachibana.masayoshi@kochi-tech.ac.jp*

Abstract: This paper presents a Common-Mode (CM) Built-In Self-Test (BIST) technique for Fully-Differential (FD) Sample-and-Hold (S/H) circuits. Based on the CM test setup, the catastrophic and parametric faults in the MOS switches and hold capacitors can be detected by checking the differential outputs, which should vary around the desired CM output of the FD Operational Amplifier (OpAmp) used in the FD S/H circuits under test. The fault simulation results in circuit-level and the layout design using Rohm 0.18-μm CMOS technology are presented to demonstrate the feasibility of the proposed CM BIST technique for FD S/H circuits.

Keywords: common-mode, fully-differential operational amplifier, sample-and-hold circuit, built-in self-test, analog mixed-signal

Classification: Integrated circuits

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1 Introduction

BIST technique has been accepted as a tool for digital verification and production test by implementing stimulus generator and response analyzer entirely on-chip. It reduces the tester complexity, eliminates the need for off-chip interfacing, and allows the device to be tested many times during the manufacturing cycle of the product [1]. Besides the design validation and postfabrication testing, BIST techniques are also used for periodic checking of circuit behaviour [2]. Hence, BIST has attracted a lot of research attention as a prospective solution for analog mixed-signal test.

FD S/H circuits are commonly used as the input stage of Analog-to-Digital Converters (ADCs) due to the elimination of clock feedthrough and charge injection, so the S/H circuits must be well tested since the faulty S/H circuits would degrade the performance of the data converter system. All S/H circuits can be tested by checking their performance parameters like acquisition time [3]. For FD S/H circuits, on-line balance self-checking [4, 5, 6] can be used. Moreover, the improved balance checking based unification of on-line and off-line test technique [2] could also be a feasible scheme for FD S/H circuits test. However, the BIST requires simple on-chip circuits to implement the test process, and these existing test techniques are difficult for FD S/H circuits BIST application. In this work, a CM BIST technique is presented for FD S/H circuit, and it can be used as input stage of ADCs and in System-on-Chip (SoC) with the proposed CM BIST circuits.

2 Common-mode test strategy

The FD OpAmp usually employs a Common-Mode Feedback (CMFB) circuit to keep the CM output at a desired value, so the CM gain significantly decreases from a_{cm} to a'_{cm} [7]:

$$a_{\mathrm{cm}} = \left.\frac{v_{\mathrm{oc}}}{v_{\mathrm{ic}}}\right|_{v_{\mathrm{id}}=0} \Rightarrow a'_{\mathrm{cm}} = \left.\frac{v_{\mathrm{oc}}}{v_{\mathrm{ic}}}\right|_{with\ \ CMFB} = \frac{a_{\mathrm{cm}}}{1 + a_{\mathrm{cms}}(-a_{\mathrm{cmc}})} \tag{1}$$

where v_{oc} and v_{ic} are the CM output and input, v_{id} is the input difference, and $a_{cms}(-a_{cmc})$ is the CM open-loop gain caused by the CMFB circuit. Additionally, the CM open-loop gain should be as high as possible in order to design a balanced-output FD OpAmp [8]. Therefore, $|a'_{cm}|$ is significantly less than $|a_{cm}|$. Moreover, the CM gain in the linearized FD OpAmp decreases to

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approximately zero [9] based on the signal flow graph modeling and analysis of the gain paths. As a result, the CM output variation caused by the variation of the CM input in the acceptable range is small due to the small CM gain.

As it can be seen from Fig. 1 (a), the flip-around S/H circuit, constructed by a FD OpAmp, can work in sample and hold modes by switching *S1*, *S2* and *S3*, which are controlled by the clock signal V_{CLK} through the non-overlapping two-phase clock generator. To form a varying CM input, V_{in1} and V_{in2} are connected and then to a shifting signal, so V_{out1} and V_{out2} should output same voltage fluctuating around the desired CM output, due to the small CM gain of the FD OpAmp with CMFB. In the sample mode, V_{CLK} is logic high, switches *S1* and *S2* are on, *S3* is off, and the FD OpAmp is operating in a unity-follower configuration with the feedback, so V_{out1} and V_{out2} are held at the desired CM output. Then V_{CLK} goes to logic low, switches *S1* and *S2* turn off, *S3* turns on, and the FD OpAmp is switched to the voltage follower configuration, so the voltage difference across each hold capacitor is kept to the voltage sampled as

$$(V_{\mathrm{in1}} - V_{\mathrm{inp}})|_{sample\ \mathrm{mode}} = (V_{\mathrm{out1}} - V_{\mathrm{inp}})|_{hold\ \mathrm{mode}} \tag{2}$$

$$(V_{\mathrm{in2}} - V_{\mathrm{inm}})|_{sample\ \mathrm{mode}} = (V_{\mathrm{out2}} - V_{\mathrm{inm}})|_{hold\ \mathrm{mode}} \tag{3}$$

Other differential points in the FD S/H circuit should also have same value ($V_{\mathrm{inp}} = V_{\mathrm{inm}}$ and $V_{\mathrm{out1}} = V_{\mathrm{out2}}$), since the inputs are connected to the test signal in the sample mode. As it was previously stated, the same voltage at V_{inp} and V_{inm} forces FD OpAmp to output two same voltages varying around the desired CM output, so the inputs V_{inp} and V_{inm} of the FD OpAmp are synchronously driven to another same value to force the FD S/H circuit to a new equilibrium under the hold mode.

In fact, the differential outputs V_{out1} and V_{out2} fluctuate around the desired CM output, but they could not be exactly equal during the CM test due to process variation and mismatch in the realistic circuit. Therefore, the proposed CM test fault signature is summarized as

$$(V_{\mathrm{CM}} - \delta_1) \leq \frac{V_{\mathrm{out1}} + V_{\mathrm{out2}}}{2} \leq (V_{\mathrm{CM}} + \delta_2) \quad \text{and} \quad |V_{\mathrm{out1}} - V_{\mathrm{out2}}| \leq \varepsilon \tag{4}$$

where V_{CM} is the desired CM output, δ_1 and δ_2 are the acceptable CM output fluctuating spaces, and ε is the acceptable maximum difference between the outputs.

The CM test can be implemented by the CM BIST setup with the test control signals shown in Fig. 1 (b). At t_1, V_{TM} starts the test by closing S_{TM} to connect the inputs (V_{in1} and V_{in2}) and outputs (V_{out1} and V_{out2}) of the FD S/H circuit under test to the output (V_{TCM}) of stimulus generator and inputs (V_{oai1} and V_{oai2}) of output analyzer, respectively. At t_2, V_{CLK} goes to high to switch the FD S/H circuit to the sample mode. Then at t_3, V_{TMC} changes to logic low to form a shifting test signal V_{TCM}. Finally, at t_4, V_{CLK} returns to low to switch S/H circuit to the hold mode. Note that V_{CLK} can use normal operation clock waveforms of the FD S/H circuit.

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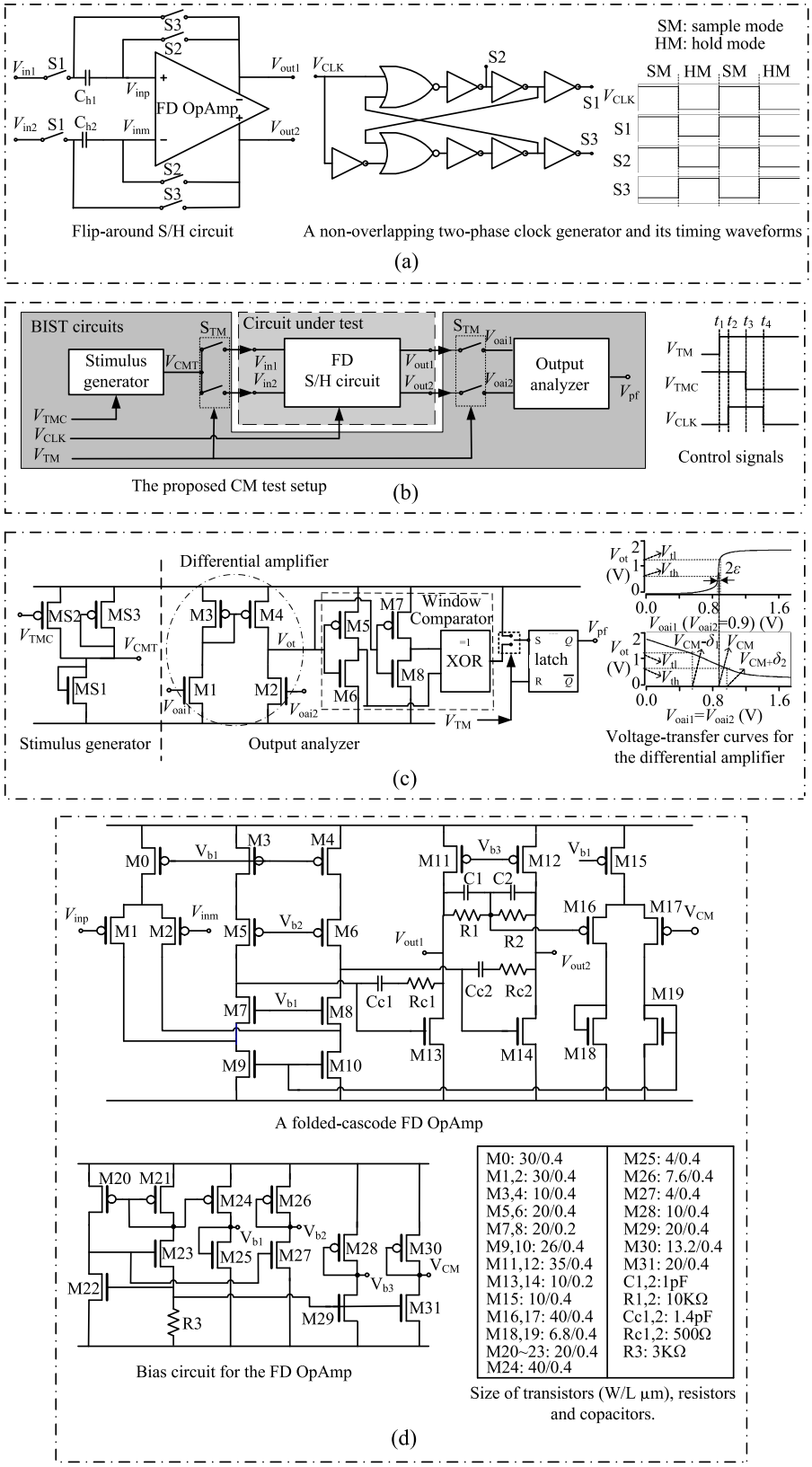

Fig. 1. (a) A flip-around FD S/H circuit and its clock generator. (b) The CM BIST setup and control signals. (c) The designed BIST circuits and voltage-transfer functions of the differential amplifier. (d) The designed folded-cascode FD OpAmp used in (a).

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3 The proposed BIST circuits

The stimulus generator and the output analyzer shown in Fig. 1 (c) were designed to implement the functions of the BIST circuits shown in Fig. 1 (b). The stimulus generator creates a transient signal V_{MCT} by switching V_{TMC}. The amplitude of V_{MCT} must be set carefully to ensure the FD OpAmp working in linear region after the new equilibrium under the hold mode. The output analyzer is composed of a differential amplifier including M1 to M4, a window comparator and a SR latch. The differential amplifier was designed to amplify the difference between the outputs of V_{out1} and V_{out2}, and their CM voltage. The shifted CM value and/or the enlarged difference of the outputs from the S/H circuit under test would derive V_{ot} to exceed the thresholds V_{tl} and V_{th} depended on the differential amplifier's differential gain and CMRR. V_{tl} and V_{th} are the V_{ot} voltages corresponding to the boundary inputs of V_{oai1} and V_{oai2}, and the boundaries are determined by the coefficients of V_{CM}, δ_1, δ_2 and ε seen in Eq. (4) from the fault-free simulation of the S/H circuit under test. The transfer is demonstrated in the voltage-transfer curves shown in Fig. 1 (c). Then the window comparator digitizes the analog output V_{ot} with reference to the new fault signature thresholds of V_{tl} and V_{th}. Finally, the added SR latch stores the appearance of a logic low voltage at the output of the XOR and to generate a final test signature V_{pf}, since some parametric faults existing in the MOS switches or hold capacitors only enlarge the difference between V_{out1} and V_{out2} at the switching moment of the control signals. Consequently, the appearance of logic high at V_{pf} means the injected fault in the FD S/H circuit can be detected.

In this work, no special test controller was designed because the FD S/H circuit under test was assumed to be one part of an analog and mixed-signal system, and the test controlling signals can be easily generated by the digital part.

4 Simulation results

In this work, the switches were implemented by transmission gates, so the incorrect R_{ON} can be modeled by the open or short in each transistor of the transmission gate. Shorts were modeled by connecting a 100 Ω resistor between each pair of terminals (gate-drain, gate-source, and drain-source). Drain and source opens were modeled by inserting a parallel combination of a 100 MΩ resistor and a 10 fF capacitor. Gate open was modeled by means of grounded parallel combination of resistor and capacitor.

To evaluate the proposed BIST technique, a flip-around FD S/H circuit was designed, including the FD OpAmp shown in Fig. 1 (d) with the desired CM output of approximately 0.9 V, the transmission gates (2/0.18 μm (W/L) for all transistors) and two hold capacitors of 0.7 pF. Fault-free simulation of the CM test setup shows that the range of the CM output of the S/H circuit is from 0.85 V to 0.94 V. Thus, based on parameters of the designed BIST circuits listed in Table I, the thresholds V_{tl} and V_{th} were designed at 0.56 V and 1.1 V with acceptable maximum difference ε of approximately 15 mV

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Table I. Parameter settings of the designed BIST circuits.

BIST Circuits Shown in Fig. 1(c)		Sizes of Elements (W/L μm)	Performances
Stimulus generator		MS1: 1.5/0.18 MS2: 0.6/0.18 MS3: 8/0.18	V_{CMT} = 0.6 V when V_{CMT} = '1' V_{CMT} = 1.5 V when V_{CMT} = '0'
Output Analyzer	Differential Amplifier	M1, M2: 10/0.8 M3, M4: 32/0.8	Differential Gain: 25.7 dB CMRR: 29.6 dB
	Window Comparator	M5: 10/0.18 M6: 0.5/0.18 M7: 0.5/0.18 M8: 5/0.18 Others: 0.54/0.18	V_{tl}: 0.56 V V_{th}: 1.1 V
	RS Latch	0.54/0.18 for all transistors	

Table II. Comparisons of this work and previous test techniques for FD S/H circuits, x = Not reported, * = Large area overhead for BIST application.

Features	Test Strategy	BIST Circuits	Fault Coverage/Area Overhead
This work	Monitor the same output with CM input	Fig. 1(c)	97%: Switches and capacitors, 90%: FD OpAmp 4%: area overhead
[3]	Performance parameters measuring	× (external device) *	× (possible full coverage)
[5]	Balance based self-checking with real working inputs	Balance checker, test stimuli *	93%: checking output voltage, 100%: improved by checking voltage stored on capacitors
[2]	Multi-differential points balance checking with frequency varying inputs	Balance checker, oscillator*	Almost full coverage for hard faults, possible full coverage for soft faults

owing to the effect of the process variation. The proposed BIST circuits were laid out using Rohm 0.18-μm CMOS technology, and caused approximately 4% area overhead.

With reference to the fault models introduced above, 66 faults for switches *S1*, *S2* and *S3*, and two faults for each capacitor were injected into the FD S/H circuit and only the pMOS gate open faults in *S3* could not be detected with the fault coverage of 97%, and more than 0.2 pF capacitance variation of the hold capacitor were detected. Additionally, 176 injected faults were detected in the total 195 faults to the FD OpAmp, resulting in approximately 90% fault coverage. Note that the faults were successively injected to the FD S/H circuit under test.

In comparison to the techniques in the works listed in Table II, the proposed BIST technique doesn't require a complex generator, and only one transient test signal can achieve high fault coverage, which reduces test cost of silicon area. The fault-free outputs of the S/H circuit under CM test should have same value, which also simplifies the output analyzer design.

5 Conclusion

The proposed CM BIST technique can detect not only catastrophic faults in the FD S/H circuits but also parametric faults of incorrect R_{on} or capacitance, and the FD OpAmp can also be tested. Thus, the proposed scheme can be an effective alternative BIST approach for FD S/H circuits in an analog mixed-signal system with high fault coverage and low test cost including

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physical area and test time.

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