Analytical Modeling and Simulation of Dual-Material Surrounding-Gate Metal–Oxide–Semiconductor Field Effect Transistors with Single-Halo Doping

2009 Jpn. J. Appl. Phys. 48 034505

(http://iopscience.iop.org/1347-4065/48/3R/034505)

Analytical Modeling and Simulation of Dual-Material Surrounding-Gate Metal–Oxide–Semiconductor Field Effect Transistors with Single-Halo Doping

Zun-Chao Li*, Rui-Zhi Zhang, and Yao-Lin Jiang

Department of Microelectronics, School of Electronics and Information Engineering, Xi'an Jiaotong University, Xi'an 710049, China

Received November 2, 2008; accepted December 6, 2008; published online March 23, 2009

We present a modified surrounding-gate metal–oxide–semiconductor field effect transistor (MOSFET), in which the gate consists of two metals with different work functions, and single-halo doping is added to the channel near the source end. The performance of the modified structure was studied by developing physics-based analytical models for the surface potential, electric field, and threshold voltage. It is shown that the novel MOSFET could significantly reduce threshold voltage roll-off and drain-induced barrier lowering, and simultaneously improve carrier transport efficiency by carefully configuring the halo doping and work functions of the dual-material gate. The results predicted using the models are compared with those obtained with the three-dimensional simulator Davinci to verify the accuracy of the proposed analytical models.

DOI: 10.1143/JJAP.48.034505

1. Introduction

To meet the demand for high speed and excellent performance of ultralarge-scale integrated (ULSI) circuits, device dimensions have been shrinking.[1,2] With the scaling down of devices, short-channel effects (SCE), drive ability degradation, and hot carrier effect (HCE) impose a physical limit on the ultimate performance of traditional planar metal–oxide–semiconductor field effect transistors (MOSFETs).[3] SCE includes threshold voltage roll-off and drain-induced barrier lowering (DIBL). Threshold voltage roll-off is a consequence of charge sharing effect, and DIBL occurs when the barrier height for channel carriers at the edge of the source is reduced owing to the effect of the drain electric field upon application of a high drain voltage. HCE is mainly caused by the strong electric field near the drain. In recent years, a number of nonclassical MOSFET structures have been proposed to extend the scalability of complementary MOS (CMOS) technology.[4–6] The surrounding-gate MOSFET by surrounding the channel completely offers the best control of SCE for a given channel length and gate oxide thickness, and is considered one of the most promising devices for downscaling below 50 nm.[7,8] Moreover, the cylindrical surrounding-gate MOSFET can suppress corner effects. However, even in the surrounding-gate MOSFET, SCE, HCE, and transconductance degradation cannot be neglected for channel lengths below 100 nm.[9]

The threshold voltage roll-off can be reduced by locally raising the channel doping next to the source or source/drain junctions. In the past few years, the local high doping concentration in the channel near the source/drain junctions has been implemented via halo or pocket implants.[10,11] Halo implants have been introduced for planar and surrounding-gate MOSFETs to adjust the threshold voltage, improve SCE, and enhance current drive capability.[12] Halo implantation devices also show flatter saturation characteristics and slightly higher breakdown voltage. As compared with symmetric halo, the single-halo structure is favorable for hot carrier reliability.[13,14] The performance improvement is dependent on the halo dose and implantation tilt angle.[14]

Dual-material gate consists of two metals in tight contact and with different work functions. The work function of the metal near the source is greater than that of the metal near the drain for a n-channel MOSFET and *vice-versa* for a p-channel MOSFET. Such a configuration provides a step in the surface-potential profile.[15,16] Because of the potential step, the potential drop and electric field peak near the drain are decreased considerably. Therefore, HCE is reduced. Moreover, the dual-material gate achieves simultaneous suppression of SCE.[17,18] Nonetheless, whether a metal can be used as the gate of MOSFETs is not only determined by its work function. It should meet the basic requirements such as thermal stability and process compatibility with dielectric deposition.[19]

To incorporate the advantages of both halo doping and dual-material gate structure, and provide more feasible choices for MOSFET process, we propose a new structure, called single-halo dual-material surrounding-gate MOSFETs (HDSM). The expressions for surface potential, electric field, and threshold voltage are derived. Subsequently, we present, using device simulation and with analytical models, the reduced SCE and HCE exhibited by HDSM. The model results are verified by comparing them with simulated results obtained using the three-dimensional device simulator Davinci of Synopsys.[20]

2. Model Formulation

The cylindrical HDSM is shown in Fig. 1. The lengths of the two metals M_1 and M_2 are L_2 and L_3–L_2, respectively. The halo length is L_1 and the halo doping concentration N_h is higher than N_c in the rest of the channel. Considering the gate structure and the halo doping, the channel can be divided into three parts.

Owing to the cylindrical symmetry of the device structure, a cylindrical coordinate system is used here, which consists of a radial direction r, a vertical direction z, and an angular component θ (not shown in the figure) in the plane vertical to the direction z. The symmetry of the structure ensures that the potential and electric field have no variation in the θ direction. Thus, a two-dimensional analysis is sufficient.

2.1 Potential model

The surface potential and electric field distribution can be

*E-mail address: zcli@mail.xjtu.edu.cn

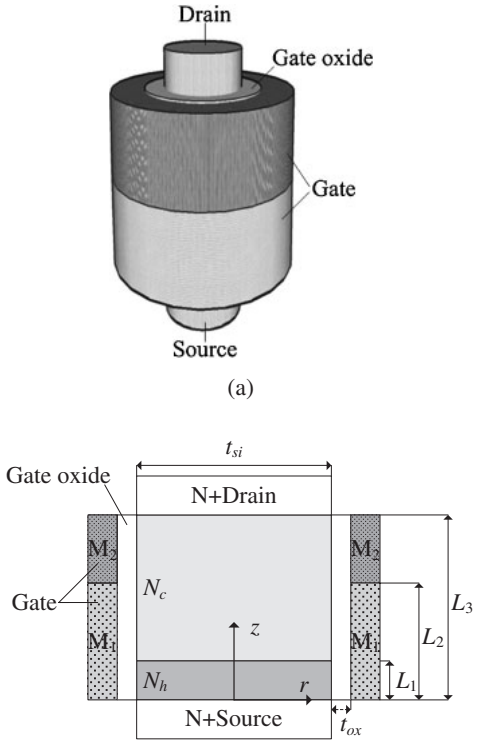

Fig. 1. Cylindrical HDSM: (a) three-dimensional device structure; (b) cross section.

derived by solving Poisson's equation in the silicon pillar. By neglecting the effect of the charge carriers and fixed oxide charges on the electrostatics of the channel, the two-dimensional Poisson's equations of potential distribution in the silicon pillar can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi_j(r,z)}{\partial r}\right)+\frac{\partial^2\phi_j(r,z)}{\partial z^2}=\frac{qN_j}{\varepsilon_{si}} \quad (L_{j-1}\le z<L_j, 0\le r\le t_{si}/2, j=1,2,3), \tag{1}$$

where ε_{si} is the dielectric constant of silicon pillar, $N_1=N_h$, $N_2=N_c$, $N_3=N_c$, $L_0=0$, $\phi_j(r,z)(j=1,2,3)$ is the potential distribution in part j.

The potential profile in the radial direction, i.e., the r-dependence of $\phi_j(r,z)$,[21] can be approximated using a simple parabolic function for the fully depleted surrounding-gate MOSFET as

$$\phi_j(r,z)=c_{j0}(z)+c_{j1}(z)r+c_{j2}(z)r^2 \quad (L_{j-1}\le z<L_j, 0\le r\le t_{si}/2, j=1,2,3), \tag{2}$$

where the arbitrary coefficients $c_{j0}(z)$, $c_{j1}(z)$, and $c_{j2}(z)(j=1,2,3)$ are functions of z only.

In HDSM, the flat band voltages of the three parts will be different and they are given as

$$V_{FB1}=\phi_1-\phi_{Sih} \tag{3a}$$

$$V_{FB2}=\phi_1-\phi_{Sic} \tag{3b}$$

$$V_{FB3}=\phi_2-\phi_{Sic}, \tag{3c}$$

where ϕ_1 and ϕ_2 are the work functions of M_1 and M_2, respectively, ϕ_{Sih} and ϕ_{Sic} are the work functions of the halo part and the rest of the silicon pillar, respectively. ϕ_{Sih} and ϕ_{Sic} are given by

$$\phi_{Sih}=\chi_{Si}+\frac{E_g}{2q}+V_T\ln\frac{N_h}{N_i}, \tag{4a}$$

$$\phi_{Sic}=\chi_{Si}+\frac{E_g}{2q}+V_T\ln\frac{N_c}{N_i}, \tag{4b}$$

where χ_{Si} is the electron affinity of silicon, E_g is the silicon band gap at 300 K, V_T is the thermal voltage, and N_i is the intrinsic carrier concentration.

The electric field in the center of the silicon pillar is zero by symmetry, so we have

$$\left.\frac{\partial\phi_j(r,z)}{\partial r}\right|_{r=0}=0=c_{j1}(z) \quad (L_{j-1}\le z<L_j, j=1,2,3). \tag{5}$$

The channel surface potential $\varphi_{sj}(z)$ is

$$\varphi_{sj}(z)=\phi(t_{si}/2,z)=c_{j0}(z)+c_{j2}(z){t_{si}}^2/4. \tag{6}$$

The electric flux at the oxide-silicon interface is continuous, so we have

$$\left.\frac{\partial\phi_j(r,z)}{\partial r}\right|_{r=t_{si}/2}=\frac{C_f}{\varepsilon_{si}}[V_{gs}-V_{FBj}-\varphi_{sj}(z)]=c_{j2}(z)t_{si} \quad (j=1,2,3), \tag{7}$$

where $C_f=2\varepsilon_{ox}/[t_{si}\ln(1+2t_{ox}/t_{si})]$, ε_{ox} is the dielectric constant of the gate oxide, t_{ox} is the thickness of the gate oxide, and V_{gs} is the gate-to-source bias voltage.

From eqs. (1)–(7), we can obtain the differential equation of the surface potential $\varphi_{sj}(z)$ as

$$\frac{d^2\varphi_{sj}(z)}{dz^2}-\lambda^2\varphi_{sj}(z)=\beta_j \quad (j=1,2,3), \tag{8}$$

where $\lambda=\sqrt{4C_f/(\varepsilon_{si}t_{si})}$ is the characteristic length and $\beta_j=qN_i/\varepsilon_{si}-\lambda^2(V_{gs}-V_{FBj})$.

Equation (8) represents three second-order differential equations with constant coefficients, and the general solution for the surface potential is

$$\varphi_{sj}(z)=A_je^{-\lambda z}+B_je^{\lambda z}-\frac{\beta_j}{\lambda^2} \quad (L_{j-1}\le z<L_j, j=1,2,3). \tag{9}$$

The coefficients A_j and B_j can be determined using the following boundary conditions.

The potential at the source end is

$$\phi_1(t_{si}/2,0)=\varphi_{s1}(0)=V_b, \tag{10}$$

where $V_b=V_T\ln(N_hN_D/N_i^2)$ is the built-in potential drop across the source–body junction and N_D is the source/drain doping concentration.

The potential at the drain end is

$$\phi_3(t_{si}/2,L_3)=\varphi_{s3}(L_3)=V_b+V_{ds}, \tag{11}$$

where V_{ds} is the applied drain–source bias voltage.

The surface potential and electric flux at the interfaces between parts 1, 2, and 3 are continuous, so we have

$$\phi_j(t_{si}/2,L_j)=\phi_{j+1}(t_{si}/2,L_j) \quad (j=1,2), \tag{12}$$

$$\left.\frac{\partial\phi_j(t_{si}/2,z)}{\partial z}\right|_{z=L_j}=\left.\frac{\partial\phi_{j+1}(t_{si}/2,z)}{\partial z}\right|_{z=L_j} \quad (j=1,2). \tag{13}$$

By using eqs. (10)–(13) and substituting L_3 with L, constants A_j and B_j can be obtained as

$$A_1 = \frac{V_{b1} + (1 - e^{\lambda L})V_{gs}}{2\sinh(\lambda L)}, \tag{14a}$$

$$B_1 = \frac{V_{b2} + (e^{-\lambda L} - 1)V_{gs}}{2\sinh(\lambda L)}, \tag{14b}$$

$$A_2 = \frac{V_{b1} + (1 - e^{\lambda L})V_{gs}}{2\sinh(\lambda L)} - \frac{e^{\lambda L_1}(U_1 - U_2)}{2}, \tag{14c}$$

$$B_2 = \frac{V_{b2} + (e^{-\lambda L} - 1)V_{gs}}{2\sinh(\lambda L)} - \frac{e^{-\lambda L_1}(U_1 - U_2)}{2}, \tag{14d}$$

$$A_3 = \frac{V_{b1} + (1 - e^{\lambda L})V_{gs}}{2\sinh(\lambda L)} - \frac{e^{\lambda L_1}(U_1 - U_2)}{2} - \frac{e^{\lambda L_2}(U_2 - U_3)}{2}, \tag{14e}$$

$$B_3 = \frac{V_{b2} + (e^{-\lambda L} - 1)V_{gs}}{2\sinh(\lambda L)} - \frac{e^{-\lambda L_1}(U_1 - U_2)}{2} - \frac{e^{-\lambda L_2}(U_2 - U_3)}{2}, \tag{14f}$$

where

$$V_{b1} = (V_b + U_1)e^{\lambda L} - (V_b + V_{ds} + U_3) - \cosh[\lambda(L - L_1)](U_1 - U_2) - \cosh[\lambda(L - L_2)](U_2 - U_3),$$

$$V_{b2} = V_b + V_{ds} + U_3 + \cosh[\lambda(L - L_1)](U_1 - U_2) + \cosh[\lambda(L - L_2)](U_2 - U_3) - (V_b + U_1)e^{-\lambda L},$$

$$U_1 = \frac{qN_h}{\lambda^2\varepsilon_{si}} + V_{FB1}, \quad U_2 = \frac{qN_c}{\lambda^2\varepsilon_{si}} + V_{FB2},$$

$$U_3 = \frac{qN_c}{\lambda^2\varepsilon_{si}} + V_{FB3}.$$

The electric field pattern along the channel determines the electron transport velocity through the channel. By differentiating $\varphi_{sj}(z)(j = 1, 2, 3)$ with respect to z, the electric field component $E_j(z)$ in the z direction is given as

$$E_j(z) = -A_j\lambda e^{-\lambda z} + B_j\lambda e^{\lambda z} \quad (L_{j-1} \le z < L_j, j = 1, 2, 3). \tag{15}$$

Equation (15) is quite useful for determining how the electric field is modified using the proposed HDSM structure.

2.2 Threshold voltage model

When the halo doping concentration N_h is greater than N_c, the minimum surface potential $\varphi_{s,min}$ lies in the halo. By differentiating $\varphi_{s1}(z)$ with respect to z and equating to zero, we can obtain the position of $\varphi_{s,min}$

$$z_{min} = \frac{1}{2\lambda}\ln\frac{A_1}{B_1}. \tag{16}$$

By substituting z_{min} for z in $\varphi_{s1}(z)$, $\varphi_{s,min}$ can be obtained as

$$\varphi_{s,min} = 2\sqrt{A_1B_1} - \beta_1/\lambda^2. \tag{17}$$

Threshold voltage V_{th} is the value of the gate voltage V_{gs} at which a conducting channel is induced at the surface of the pillar. Therefore, the threshold voltage is taken to be that value of V_{gs} at which $\varphi_{s,min} = 2\varphi_F$, where φ_F is the difference between the Fermi level in the halo part and the intrinsic Fermi level. From eqs. (14) and (17), we have

$$V_{th} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma}, \tag{18}$$

where

$$\sigma = 2\cosh(\lambda L) - 2 - \sinh^2(\lambda L),$$

$$\eta = V_{b1}(e^{-\lambda L} - 1) + V_{b2}(1 - e^{\lambda L}) + 2\sinh^2(\lambda L)(2\varphi_F + U_1),$$

and

$$\xi = V_{b1}V_{b2} - \sinh^2(\lambda L)(2\varphi_F + U_1)^2.$$

3. Results and Discussion

Now, we will examine the performance of HDSM in terms of threshold voltage roll-off, DIBL, and carrier transport efficiency. We will also compare the performance of HDSM with dual-material surrounding-gate MOSFETs (DSMs) and single-halo surrounding-gate MOSFETs (HSMs). We will also verify the analytical models by comparing the analytical results with the simulated data obtained using Davinci. Unless otherwise noted, drain and source doping concentration $N_D = 10^{20}\,cm^{-3}$, $N_h = 3 \times 10^{17}\,cm^{-3}$, $N_c = 4 \times 10^{16}\,cm^{-3}$, $t_{ox} = 4\,nm$, $t_{si} = 50\,nm$, $L_1 = 25\,nm$, $L_2 = 60\,nm$, $L = 100\,nm$, and the work functions of M_1 and M_2 are 4.5 and 4.1 V, respectively.

The surface potential distributions of HDSM, DSM, and HSM along the channel are plotted in Fig. 2. It can be seen from the figure that the minimum surface potential occurs in the halo part for HDSM. For HDSM, there is an extra potential step on the right of the minimum surface potential as compared with DSM, and there exists an additional potential step near the boundary of the two metals as compared with HSM. The height of the steps will increase with the increase in the halo doping and the difference between the work functions of the two metals. Because of the two potential steps, HDSM can improve SCE, HCE, and current drive capability more effectively than DSM and HSM.

The surface electric field in the channel is shown in Fig. 3. It could be found that there is an additional electric field peak near the halo boundary in HDSM as compared with DSM, and there is also one extra electric field peak near the interface of the two metals as compared with HSM. Thus,

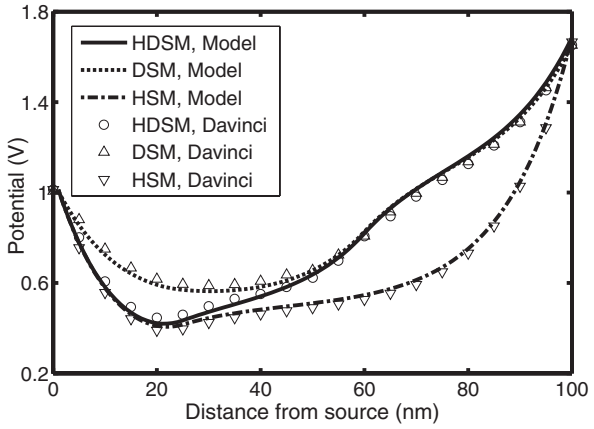

Fig. 2. Surface potential along the channel (V_{gs} = 0.2 V, V_{ds} = 0.6 V).

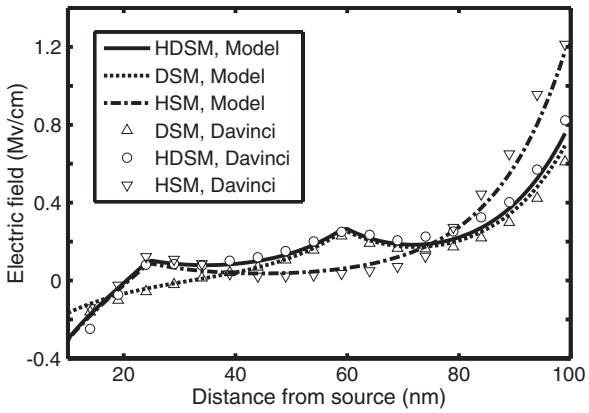

Fig. 3. Surface electric field along the channel (V_{gs} = 0.2 V, V_{ds} = 0.6 V).

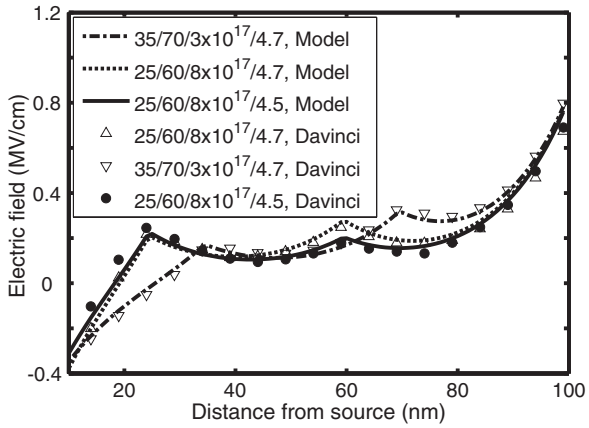

Fig. 4. Surface electric field of HDSM with different halo and gate configurations (V_{gs} = 0.2 V, V_{ds} = 0.6 V).

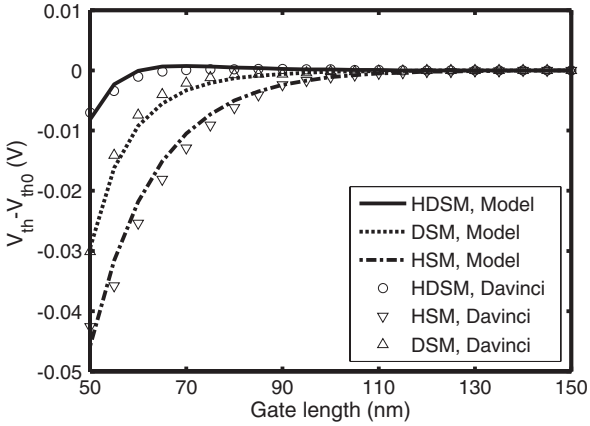

Fig. 5. Threshold voltage roll-off with gate length.

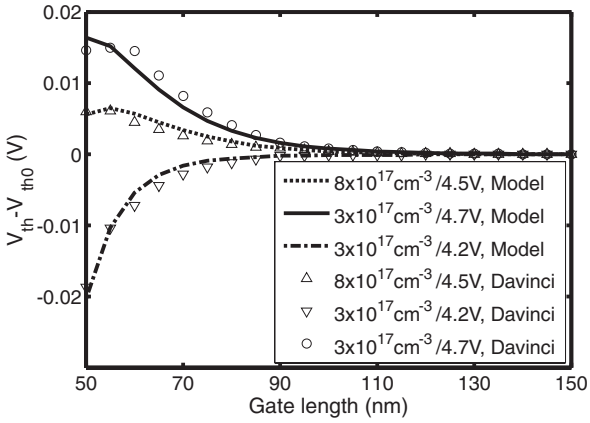

Fig. 6. Threshold voltage roll-off of HDSM with different halo and gate configurations.

carriers will be accelerated more in HDSM than in DSM and HSM. Carrier transport efficiency and therefore current drive capability are increased in HDSM. It can also be seen that the electric field near the drain is lower in HDSM than in HSM. Therefore, HDSM exhibits further suppression of HCE than HSM.

Figure 4 shows the surface electric field of HDSM with different halo and gate configurations. In each legend, the values represent the length L_1 of the halo in nm, the length L_2 of M_1 in nm, the halo doping concentration N_h in cm^{-3}, and the work function ϕ_1 of M_1 in V. It is indicated in the figure that increasing the halo length makes the first electric field peak move away from the source, thereby delaying the speeding-up of carriers. Increasing the halo doping concentration increases the first electric field peak, thereby enhancing the speeding-up of carriers. Increasing the work function of M_1 increases the second electric field peak, thereby enhancing the speeding-up of carriers. Increasing the length of M_1 makes the second electric field peak move toward the drain, thereby delaying the speeding-up of carriers. However, changing the halo and gate configurations has no clear effect on the electric field near the drain, and therefore no clear effect on HCE.

Figure 5 shows the threshold voltage roll-off with gate length, where V_{th0} is the V_{th} value with a gate length of 150 nm. It shows that because of the double suppression effects of the dual-material gate and halo in HDSM, its threshold voltage roll-off is much smaller than those of DSM and HSM. The threshold voltage variation of HDSM remains very small when the gate length is over 55 nm. This feature is very important when the device dimensions are continuously shrinking. With decreasing channel lengths, it is very difficult to obtain precise channel length across the wafer. However, a threshold voltage variation from device to device is least desirable.

Figure 6 shows the threshold voltage roll-off variation with gate length of HDSM with different halo and dual-material gate configurations. By combining Figs. 5 and 6, it is observed that with the increase in the work function of M_1 and halo doping concentration, the suppression capability of the threshold voltage roll-off of the device is increased. The device could even exhibit reverse SCE. That is, the threshold voltage will go up with the decrease in gate length when the work function of M_1 and the halo doping concentration reach certain values. Thus, to make the DIBL of HDSM as low as possible, we need to optimize the configuration of the halo doping and the work function difference of the dual-material gate. HDSM also provides more flexible process choices for making MOSFET with low voltage roll-off.

DIBL can be expressed as $\Delta V_{th}/\Delta V_{ds}$. DIBL variations of HDSM, DSM, and HSM with gate length are presented in Fig. 7, where $\Delta V_{th} = V_{th}|_{V_{ds}=0} - V_{th}|_{V_{ds}=2}$ and $\Delta V_{ds} = 2$ V.

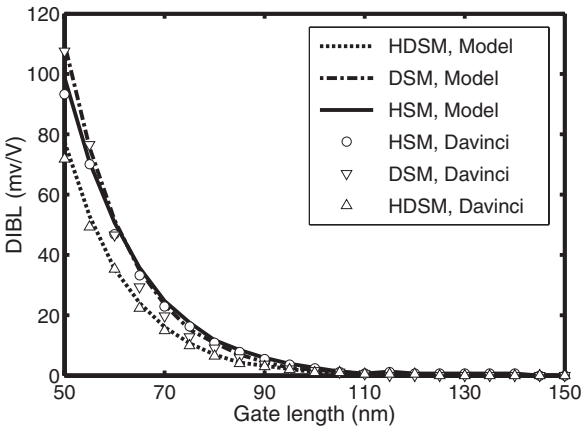

Fig. 7. DIBL variation with gate length.

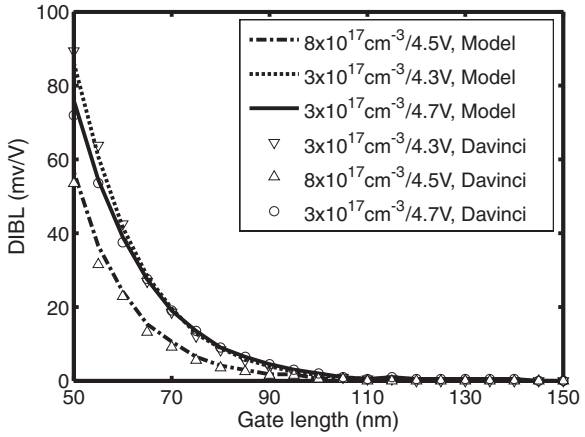

Fig. 8. DIBL of HDSM with different halo and gate configurations.

It is clear from the figure that because of the joint effects of the halo and dual-material gate, HDSM shows much better suppression of DIBL than DSM and HSM.

Figure 8 shows the DIBL variation of HDSM with different halo doping and gate configurations. By combining Figs. 8 and 7, it can be observed that DIBL of HDSM does not vary monotonically with the work function of M_1 when the halo doping concentration remains constant. However, DIBL decreases with increasing halo doping concentration. Thus, careful optimization of the work function difference of the dual-material gate should be carried out to obtain HDSM with as small DIBL as possible at a given halo doping level.

Figures 2 to 8 show that the analytical models are in good agreement with the results obtained using Davinci.

4. Conclusions

Single-halo and dual-material gate structures are used in the surrounding-gate MOSFET to extend its scalability. Two-dimensional analytical models of the surface potential, surface electric field, and threshold voltage are derived for the novel MOSFET, HDSM. The results obtained from the models agree well with the simulated results obtained using Davinci. It is shown that HDSM exhibits better performance than the dual-material surrounding-gate MOSFET and the surrounding-gate MOSFET. The two electric field peaks near the halo boundary and the interface of the two metals make carriers travel through the channel more quickly. Threshold voltage roll-off and drain-induced barrier lowering of HDSM can be suppressed effectively by carefully configuring the halo doping and the work functions of the dual-material gate. HDSM provides more flexible process choices for optimizing the performance of MOSFETs.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grant No. 10771168), the State Key Development Program for Basic Research of China (Grant No. 2005CB321701), and Natural Science Basic Research Plan in Shaanxi Province of China (Grant No. SJ08-ZT13).

1) S. Bhattacherjee and A. Biswas: Semicond. Sci. Technol. **23** (2008) 015010.
2) H. Kaur, S. Kabra, S. Bindra, S. Haldar, and R. S. Gupta: Solid-State Electron. **51** (2007) 398.
3) S. Oh, D. Monroe, and J. M. Hergenrother: IEEE Electron Device Lett. **21** (2000) 445.
4) Y. Li and H.-M. Chou: IEEE Trans. Nanotechnol. **4** (2005) 645.
5) J. T. Park, J. P. Colinge, and C. H. Diaze: IEEE Electron Device Lett. **22** (2001) 405.
6) H. A. E. Hamid, J. R. Guitart, V. Kilchytska, D. Flandre, and B. Iñiguez: IEEE Trans. Electron Devices **54** (2007) 2487.
7) J. P. Colinge: Microelectron. Eng. **84** (2007) 2071.
8) B. Yu, W. Lu, H. Lu, and Y. Taur: IEEE Trans. Electron Devices **54** (2007) 492.
9) L. Risch: Solid-State Electron. **50** (2006) 527.
10) S. Zanchetta, A. Todon, A. Abramo, L. Selmi, and E. Sangiorgi: Solid-State Electron. **46** (2002) 429.
11) H. V. Meer and K. D. Meyer: IEEE Trans. Electron Devices **48** (2001) 2292.
12) Z. C. Li: Chin. Phys. B **17** (2008) 4312.
13) A. Bansal and K. Roy: IEEE Trans. Electron Devices **52** (2005) 397.
14) D. Song, J. Lim, K. Lee, Y. Park, and H. Min: Solid-State Electron. **39** (1996) 923.
15) M. J. Kumar and A. Chaudhry: IEEE Trans. Electron Devices **51** (2004) 569.
16) K. Goel, M. J. Saxena, M. Gupta, and R. S. Gupta: IEEE Trans. Electron Devices **52** (2005) 23.
17) X. Zhou and W. Long: IEEE Trans. Electron Devices **45** (1998) 2546.
18) A. Chaudhry and M. J. Kumar: IEEE Trans. Electron Devices **51** (2004) 1463.
19) V. Misra, H. Zhong, and H. Lazar: IEEE Electron Device Lett. **23** (2002) 354.
20) Davinci User Guide (Synopsys Inc., 2005).
21) M. J. Kumar, A. A. Orouji, and H. Dhakad: IEEE Trans. Electron Devices **53** (2006) 920.