An Improved ZVS PWM Three-Level Converter

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***Abstract*—This paper proposes an improved zero-voltage-switching pulse-width-modulation three-level converter (ZVS PWM TL converter), which is improved from the original ZVS PWM TL converter just by exchanging the position of the resonant inductor and the transformer, such that the transformer is connected with the lagging switches. The improved converter has several advantages over the original one, e.g., the clamping diodes conduct only once in a switching period, and the resonant inductor current is smaller in zero state, leading to a higher efficiency and reduced duty cycle loss. A blocking capacitor is usually introduced to the primary side to prevent the transformer from saturating, this paper analyzes the effects of the blocking capacitor in different positions, and a best scheme is determined. A 2.5-kW prototype converter verifies the effectiveness of the improved converter and the best scheme for the blocking capacitor.**

***Index Terms*—Clamping diode, pulse-width-modulation, three-level converter, zero-voltage-switching.**

I. Introduction

THE main advantage of the three-level converter (TL converter) is that the voltage stress on the switches is only half that of the input voltage. Thus, the TL converter is well suited for the high voltage and high power dc-to-dc conversion [1], [2]. A zero-voltage-switching pulse-width-modulation TL converter (ZVS PWM TL converter) realize ZVS for the switches with the use of a leakage inductor and the output capacitors of the switches [3], however, the rectifier diodes suffer reverse recovery. This results in oscillation and voltage spikes. In order to solve this problem, [4] introduced two clamping diodes to the basic TL converter to eliminate the oscillation and clamp the rectified voltage to the reflected input voltage. Its main circuit and key waveforms are shown in Fig. 1.

However, ZVS PWM TL converter with two clamping diodes has several disadvantages as follow: 1) At zero state, resonant inductor is shorted by the clamping diode, which results in increasing conduction loss; 2) The clamping diode conducts twice in a cycle, and one of the conduction is useless for clamping; 3) A blocking capacitor is usually introduced to the primary side to prevent the transformer from saturating. This leads to asymmetry of the resonant inductor current or transformer current.

In order to solve these problems, this paper show how to improve the converter by just exchanging the position of the resonant inductor and the transformer, such that the transformer is connected with the lagging switches. The improved converter, shown in Fig. 2, has several advantages over the original one, e.g., the clamping diodes conduct only once in a switching period, and the resonant inductor current is smaller in zero state, leading to higher efficiency and reduced duty cycle loss.

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II. Operation Principle

Figs. 1 and 2 show two ZVS PWM TL converters with clamping diode, respectively. $Q_1 \sim Q_4$ are the main power switches, $D_1 \sim D_4$ are the body diodes of $Q_1 \sim Q_4$, $C_1 \sim C_4$ are the output capacitors of $Q_1 \sim Q_4$, and L_r is the external resonant inductor to realize ZVS for the inner switches. C_{ss} is the flying capacitor, its voltage in steady state is $V_{in}/2$. D_5 and D_6 are the freewheeling diodes (also called "clamping diodes" in three-level inverters and multi-level inverters), which help stabilize the voltage across C_{ss}. D_7 and D_8 are clamping diodes. Phase-shifted (PS) modulation strategy is employed in the ZVS TL converter, Q_1 and Q_4 are the leading switches and Q_2 and Q_3 are the lagging switches.

Fig. 1(a) shows that T_r is connected with leading switches through D_5 and D_6, and we define it as T_r-lead Type, which is the original converter; Fig. 2(a) shows that T_r is connected with lagging switches, and we define it as T_r-lag Type. This is the improved converter. The operation principle of T_r-lead Type had been analyzed in [4], and T_r-lag Type will be analyzed as follows.

Before the analysis, we make the following assumptions: 1) all the switches and diodes are ideal, except for the rectifier diodes D_{R1} and D_{R2}, which is equivalent to an ideal diode and a paralleled capacitor to simulate the reverse recovery; 2) all the inductors, capacitors and transformer are ideal; 3) $C_1 = C_4 = C_{\text{lead}}$, $C_2 = C_3 = C_{\text{lag}}$; 4) $L_f \gg L_r/K^2$, where K is the windings ratio of the primary and secondary windings; 5) C_{d1} and C_{d2} are equal and large enough to be treated as two voltage sources with voltage equal to the half of the input voltage V_{in}, i.e., $V_{cd1} = V_{cd2} = V_{in}/2$.

A. Mode 0 [Prior to t_0] [Refer to Fig. 3(a)]

Prior to t_0, Q_1 and Q_2 are conducting, D_{R1} is conducting and D_{R2} is off.

B. Mode 1 $[t_0, t_1]$ [Refer to Fig. 3(b)]

Q_1 is turned off at t_0, the primary current i_p charges C_1 and discharges C_4 via C_{ss}, v_{AB} decays. Because of $L_r \ll K^2 L_f$, v_{Lr} is nearly to zero and the potential voltage of C is nearly to $V_{in}/2$. D_7 does not conduct in this mode. Due to v_{AC} decays, the secondary voltage of the transformer decays correspondingly, thus, C_{DR2} is discharged. Therefore, the filter inductor current is divided into two parts: the larger part is reflected to the primary to charges C_1 and discharges C_4, the smaller part discharges C_{DR2}. The further simplified equivalent circuit of

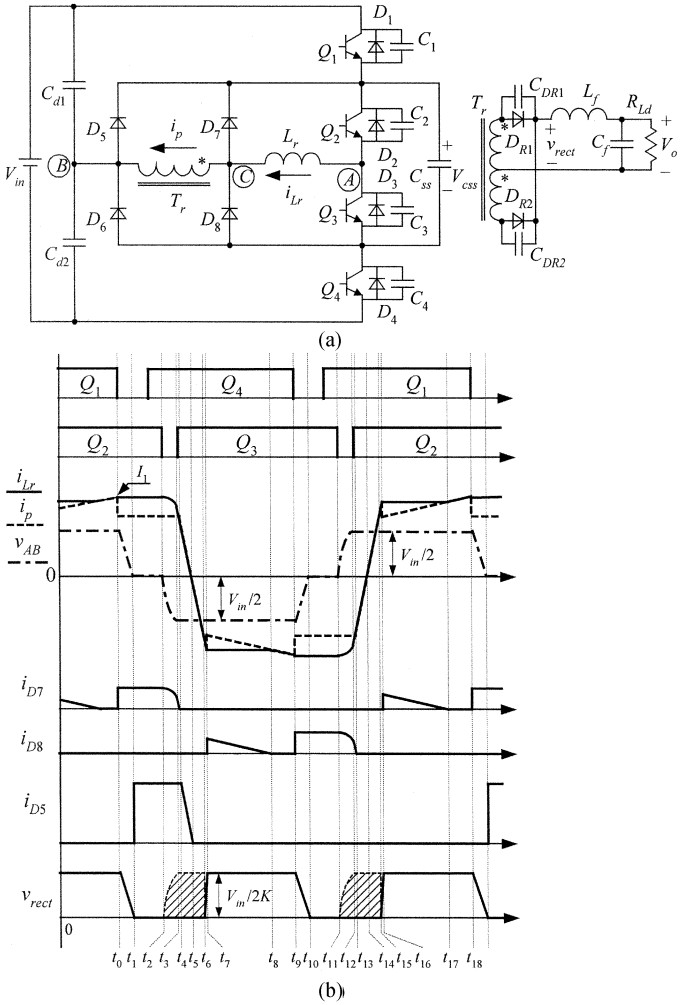

Fig. 1. The original ZVS PWM TL converter. (a) Main circuit. (b) Key waveforms.

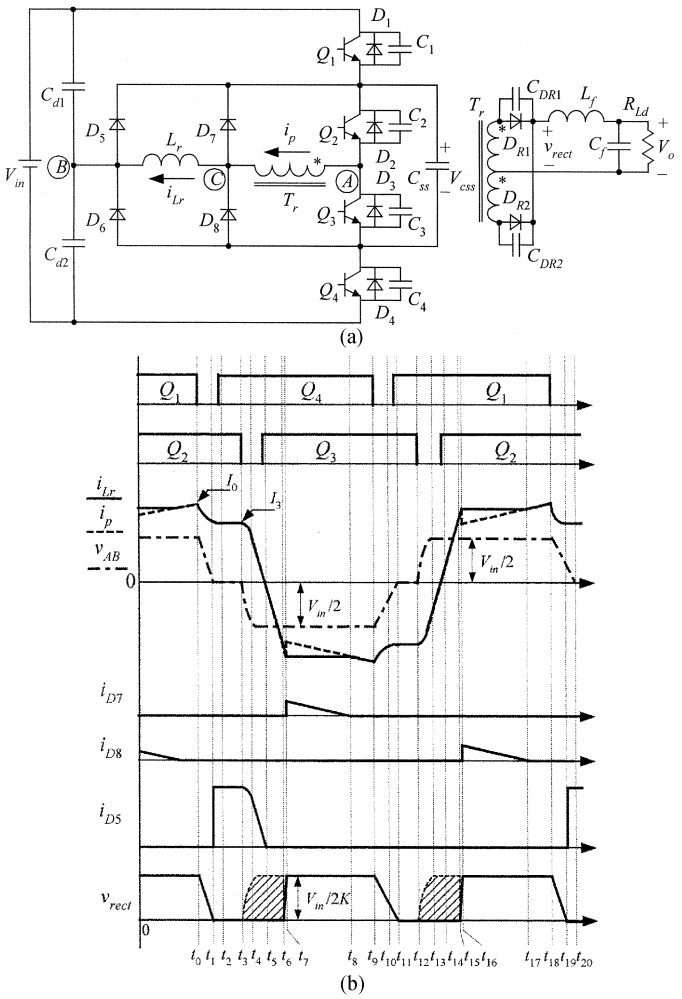

Fig. 2. The improved ZVS PWM TL converter. (a) Main circuit. (b) Key waveforms.

mode 1 is shown in Fig. 4(a), where C'_D is the reflected capacitor of C_{DR2} to the primary, I_0 is the value of primary current at t_0 which equals to the reflected filter inductor current

$$v_{C1}(t) = \frac{C'_D}{2C_{\text{lead}}(2C_{\text{lead}} + C'_D)\omega_1} I_0 \sin\omega_1(t - t_0) + \frac{1}{2C_{\text{lead}} + C'_D} I_0(t - t_0) \quad (1)$$

$$v_{C4}(t) = \frac{V_{in}}{2} - v_{C1}(t) \quad (2)$$

$$v_{C'_D}(t) = \frac{V_{in}}{2} - \frac{1}{2C_{\text{lead}} + C'_D} I_0(t - t_0) + \frac{1}{(2C_{\text{lead}} + C'_D)\cdot\omega_1} I_0 \sin\omega_1(t - t_0) \quad (3)$$

$$i_p(t) = i_{Lr}(t) = \frac{2C_{\text{lead}}}{2C_{\text{lead}} + C'_D} I_0 + \frac{C'_D}{2C_{\text{lead}} + C'_D} I_0 \cos\omega_1(t - t_0) \quad (4)$$

where $\omega_1 = \sqrt{(2C_{\text{lead}} + C'_D)/(2C_{\text{lead}} \cdot C'_D \cdot L_r)}$.

C. Mode 2 $[t_1, t_2]$ *[Refer to Fig. 3(c)]*

As D_4 is conducting, the voltage of C_4 is clamped at zero, so Q_4 is turned on at zero-voltage condition. C_{DR2} is discharging and i_{Lr} and i_p decay. The further simplified equivalent circuit of mode 2 is shown in Fig. 4(b)

$$i_p(t) = i_{Lr}(t) = (I_1 - I_0)\cos\omega_2(t - t_1) - \frac{V_{C'_D}(t_1)}{L_r\omega_2}\sin\omega_2(t - t_1) + I_0 \quad (5)$$

$$v_{C'_D}(t) = \frac{1}{C'_D \cdot \omega_2}(I_1 - I_0)\sin\omega_2(t - t_1) + V_{C'_D}(t_1)\cos\omega_2(t - t_1) \quad (6)$$

where $\omega_2 = \sqrt{1/(L_r \cdot C'_D)}$, I_1 is the value of i_p at t_1.

D. Mode 3 $[t_2, t_3]$ *[Refer to Fig. 3(d)]*

At t_2, v_{CDR2} decays to zero and D_{R2} conduct. The potential voltage of C decays to $V_{in}/2$, i_p and i_{Lr} are freewheeling and keep unchanged.

E. Mode 4 $[t_3, t_4]$ *[Refer to Fig. 3(e)]*

Q_2 is turned off at t_3, i_{Lr} charges C_2 and discharges C_3 via C_{ss}. Due to C_2, Q_2 is zero-voltage turn-off. At this time $v_{AB} = -v_{C2}$, both D_{R1} and D_{R2} conduct simultaneously,

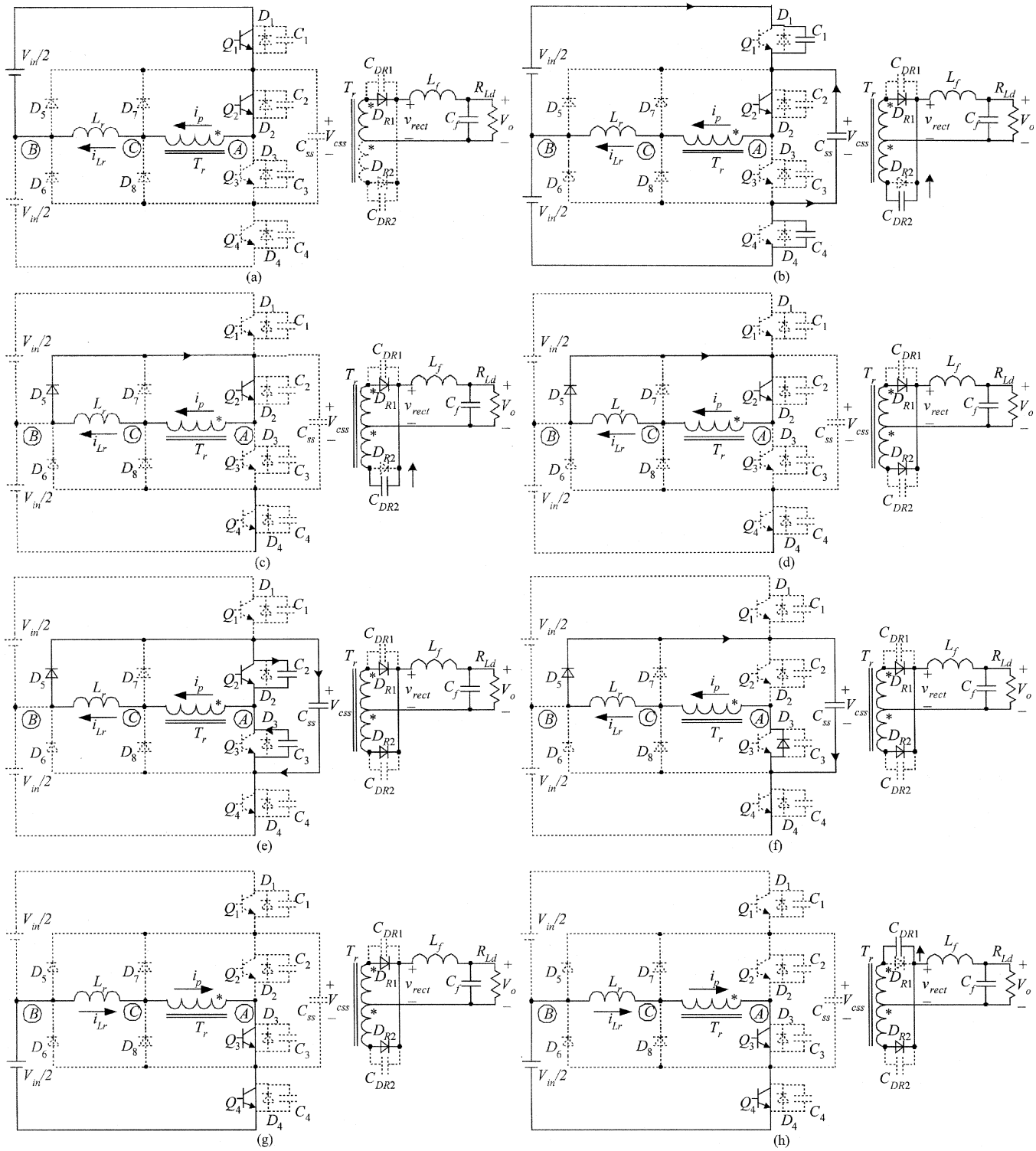

Fig. 3. The equivalent circuits of each switching mode. (a) Prior To t_0. (b) $[t_0, t_1]$. (c) $[t_1, t_2]$. (d) $[t_2, t_3]$. (e) $[t_3, t_4]$. (f) $[t_4, t_5]$. (g) $[t_5, t_6]$. (h) $[t_6, t_7]$.

which clamps both the primary and secondary voltage at zero, so v_{AB} is fully applied on L_r. L_r resonates with C_2 and C_3 during this mode

$$i_{Lr}(t) = i_p(t) = I_3 \cos \omega_3 (t - t_2) \tag{7}$$

$$v_{C4}(t) = Z_{r1} I_3 \sin \omega_3 (t - t_2) \tag{8}$$

$$v_{C2}(t) = \frac{V_{in}}{2} - Z_{r1} I_3 \sin \omega_3 (t - t_2) \tag{9}$$

where $Z_{r1} = \sqrt{L_r / 2C_{\text{lag}}}$, $\omega_3 = 1/\sqrt{2 L_r C_{\text{lag}}}$, I_3 is the value of i_p at t_3.

At t_4, v_{C2} rises to $V_{in}/2$ and v_{C3} decays to zero.

F. Mode 5 $[t_4, t_5]$ [Refer to Fig. 3(f)]

D_3 conducts naturally at t_4, so Q_3 can be turned on at zero-voltage condition. As i_p is not enough to provide the load current, both the two rectifier diodes conduct, which clamps both

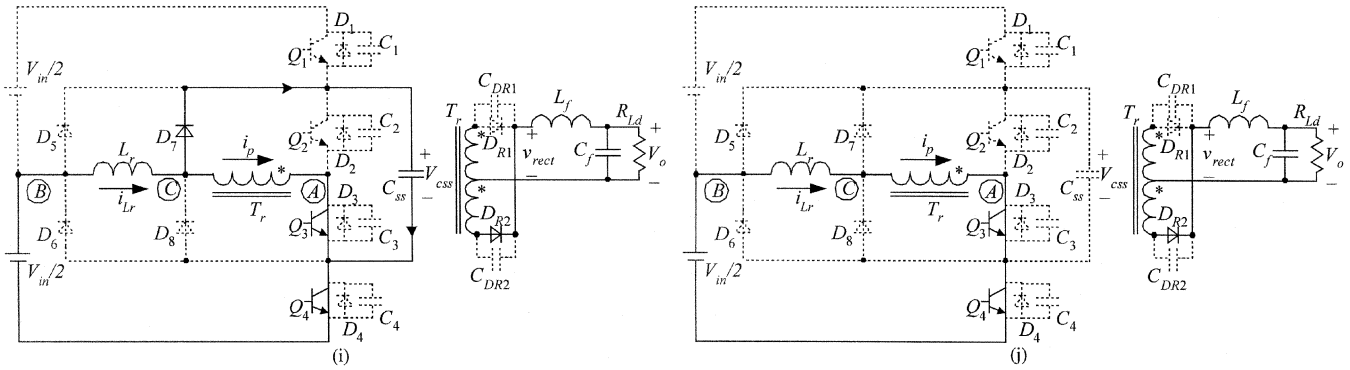

Fig. 3. (*Continued.*) The equivalent circuits of each switching mode. (i) $[t_7, t_8]$. (j) $[t_8, t_9]$.

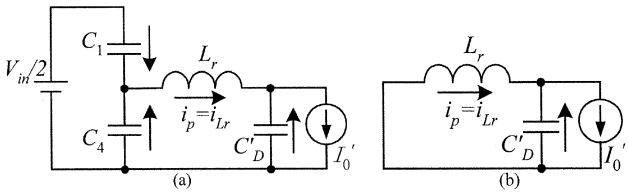

Fig. 4. Further simplified equivalent circuit of mode 1 and mode 2. (a) Mode 1. (b) Mode 2.

the primary and secondary voltage at zero, D_5 continue conducting, $V_{in}/2$ is applied on L_r, which makes i_{Lr} decays linearly

$$i_{Lr}(t) = i_p(t) = I_4 - \frac{V_{in}}{2L_r}(t - t_4) \tag{10}$$

where I_4 is the value of i_p at t_4.

G. Mode 6 $[t_5, t_6]$ *[Refer to Fig. 3(g)]*

From t_5, i_p continues rising in the negative direction and flows through Q_3 and Q_4. As i_p is still not enough to provide the load current, both the two rectifier diodes conduct, and both the primary and secondary voltage are zero, $V_{in}/2$ is applied on L_r, which makes i_{Lr} and i_p rise linearly in the negative direction

$$i_{Lr}(t) = i_p(t) = -\frac{V_{in}}{2L_r}(t - t_5) \tag{11}$$

where I_5 is the value of i_p at t_5.

H. Mode 7 $[t_6, t_7]$ *[Refer to Fig. 3(h)]*

At t_6, i_p rises to the reflected filter inductance current $-i_{Lf}(t_6)/K$, D_{R1} turns off, all the output current flows through D_{R2}

$$i_p(t) = i_{Lr}(t) = \frac{I_{Lf}(t_6)}{K} + \frac{V_{in}}{2Z_{r2}} \sin \omega_4 (t - t_6) \tag{12}$$

$$v_{\mathrm{CDR1}}(t) = \frac{V_{in}}{K}[1 - \cos \omega_4 (t - t_6)] \tag{13}$$

where $Z_{r2} = \sqrt{L_r / C'_D}$, $\omega_4 = 1/\sqrt{L_r C'_D}$.

At t_7, the voltage of C_{DR1} reaches to V_{in}/K, and the primary voltage v_{CA} reaches to $-V_{in}/2$, which forces D_7 to conduct, therefore, the voltage of C_{DR1} is clamped at V_{in}/K

$$I_{Lr}(t_7) = I_p(t_7) = -\left[\frac{I_{Lf}(t_6)}{K} + \frac{V_{in}}{2Z_{r2}}\right]. \tag{14}$$

I. Mode 8 $[t_7, t_8]$ *[Refer to Fig. 3(i)]*

As D_7 conducts, i_p has a downward step to the reflected filter inductance current, and i_{Lr} keeps unchanged. The small difference between i_p and i_{Lr} flows through D_7

$$i_p(t) = -\frac{\frac{V_{in}}{2} - KV_o}{K^2 L_f} \cdot (t - t_7). \tag{15}$$

At t_8, i_p equals to i_{Lr}, D_7 turns off naturally.

J. Mode 9 $[t_8, t_9]$ *[Refer to Fig. 3(j)]*

During this mode, the primary side powers the load, i_p equals to i_{Lr} expressed as (15).

At t_9, turn off Q_4, starting the second half cycle $[t_9, t_{18}]$, which is similar to the first half cycle $[t_0, t_9]$.

III. The Conditions of ZVS and Duty Cycle Loss

A. The Condition of ZVS for the Leading Switches

From mode 1, in order to realize ZVS for the leading switches, it needs enough energy to charge C_1 and discharge C_4 and C_{DR2}, i.e.,

$$\begin{aligned} E_{\mathrm{lead}} &> \frac{1}{2}C_1\left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2}C_4\left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2}C'_D\left(\frac{V_{in}}{2}\right)^2 \\ &= C_{\mathrm{lead}}\left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2}C'_D\left(\frac{V_{in}}{2}\right)^2. \end{aligned} \tag{16}$$

As C_{oss}, the output capacitor of MOSFET, is nonlinear and inversely proportional to the square root of the voltage, it will be

multiplied by a factor 4/3 to approximate the correct average capacitance value with a varying V_{DS}[5], i.e., $C_{\text{lead}} = (4/3)C_{oss}$, so (16) is changed to the (17).

$$E_{\text{lead}} > \frac{4}{3}C_{oss}\left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2}C'_D\left(\frac{V_{in}}{2}\right)^2. \tag{17}$$

The energy is provided by the resonant inductor and filter inductor. As filter inductor is quite large, its energy is large enough to realize ZVS for the leading switches in a wide load range.

B. The Condition of ZVS for the Lagging Switches

From mode 4, in order to realize ZVS for the lagging switches, it needs enough energy to discharge C_3 and charge C_2, i.e.,

$$\begin{aligned} E_{\text{lag}} &> \frac{1}{2}C_2\left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2}C_3\left(\frac{V_{in}}{2}\right)^2 \\ &= C_{\text{lag}}\left(\frac{V_{in}}{2}\right)^2 = \frac{4}{3}C_{oss}\left(\frac{V_{in}}{2}\right)^2. \end{aligned} \tag{18}$$

The energy is only provided by the resonant inductor, i.e.,

$$\frac{1}{2}L_r I_p^2(t_3) > \frac{4}{3}C_{oss}\left(\frac{V_{in}}{2}\right)^2. \tag{19}$$

As the resonant inductance is quite smaller than the reflected filter inductance, the lagging switch is more difficult to realize ZVS than the leading switch. The leakage inductance of transformer is small, and could not provide the enough energy. Therefore, in order to realize ZVS for the lagging switch in a relatively wide load range, we should add a resonant inductance.

C. The Duty Cycle Loss

The resonant inductance limits the rise (or decay) slope of i_p, so it needs time for i_p to transit from the positive (or negative) direction to the negative (or positive) reflected filter inductance current, i.e., $[t_3, t_6]$ and $[t_{12}, t_{15}]$ as shown in Fig. 2(b). During $[t_3, t_6]$ and $[t_{12}, t_{15}]$, v_{AB} is $+V_{in}/2$ or $-V_{in}/2$, but i_p is not enough to provide the output current, both the rectifier diodes conduct, which makes the secondary rectified voltage v_{rect} be zero, thus, v_{rect} loses the voltage in $[t_3, t_6]$ and $[t_{12}, t_{15}]$ as the shadow area shown in Fig. 2(b).

The time of the lost voltage is $[t_3, t_6]$, the duty cycle loss is the ratio between t_{36} and the half of the switching period, i.e.,

$$D_{\text{loss}} = \frac{t_{36}}{\frac{T_s}{2}} = \frac{4L_r \cdot [I_p(t_3) + I_p(t_6)]}{V_{in} \cdot T_s}. \tag{20}$$

$I_p(t_3)$ can be calculated by (1)–(6), and $I_p(t_6)$ is I_o/K approximately. From (20), we know that: 1) the larger L_r is, the larger D_{loss} is; 2) the larger load current is, the larger D_{loss} is; 3) the lower V_{in} is, the larger D_{loss} is.

IV. Comparison Between T_r-Lead Type and T_r-Lag Type

According to the above analysis, we know that T_r-lag Type converter can eliminate voltage oscillation resulting from the reverse recovery of the rectifier diodes, just as the T_r-lead Type converter can.

The difference between the two is the turn-off of the leading switches. When the leading switch is turned off in the T_r-lead Type converter, the clamping diode conducts, and the resonant inductor is shorted. Its current stays at $I_p(t_1)$ until the turn-off of the lagging switch [4]. When the leading switch in the T_r-lag Type converter is turned off, the clamping diode does not conduct, and the resonant inductor current equals to the primary current, and they both decay to $I_p(t_3)$, $I_p(t_3) < I_p(t_1)$. Table I shows the comparison between T_r-lead Type and T_r-lag Type converter.

A. Achievement of ZVS

In order to achieve ZVS for the leading switches, the T_r-lead Type converter needs enough energy to charge/discharge the output capacitors of the leading switches and discharge the junction capacitor of the rectifier diode. The energy is provided only by the filter inductance. For the T_r-lag Type converter to achieve ZVS for the leading switchers, it needs enough energy to charge/discharge the output capacitors of the leading switches and discharge part of the junction capacitor of the rectifier diode, and the energy is provided by the filter inductor and resonant inductor. Therefore, it is slightly easier to achieve ZVS for the T_r-lag Type converter than the T_r-lead Type converter.

The resonant inductor provides energy to achieve ZVS for the lagging switches in both converters. When the lagging switch turns off, the resonant inductor current is smaller in the T_r-lag Type converter than that in the T_r-lead Type converter, so it is slightly more difficult for the lagging switches to achieve ZVS in the T_r-lag Type converter than in the T_r-lead Type converter.

B. Current of the Clamping Diodes

As the clamping diodes conduct only once in a switching cycle in T_r-lag Type converter, the current rating of the clamping diodes can be reduced.

C. Conduction Loss in Zero State

In zero state, the resonant inductor current is smaller in T_r-lag Type converter than that of T_r-lead Type converter, so the conduction loss of the resonant inductor and the primary side is reduced, leading to a higher efficiency.

D. Duty Cycle Loss

The duty cycle loss is proportional to the time for the resonant inductor current to transit from the positive (or negative) value to the negative (or positive) reflected output filter inductor current. As the initial transition current of resonant inductor is smaller in T_r-lag Type converter than that of the T_r-lead Type converter, the duty cycle loss is reduced, so the primary to secondary windings ratio of the transformer can be increased, thus, the time of the zero state will be shortened and the primary current is reduced. As a result, the conduction loss in zero state will be further reduced, a higher efficiency can be expected, especially for a wide line range.

From the comparison above, it can be seen that the T_r-lag Type converter has more advantages than the T_r-lead Type converter.

V. Simplified T_r-Lag Type

By observing Fig. 2, we can see that the freewheeling diode D_5 conducts only during $[t_1, t_5]$ [see Fig. 3(c)-(f)]. As C_{ss} is

TABLE I
COMPARISON BETWEEN T_r-LEAD TYPE AND T_r-LAG TYPE

	T_r-lead Type	T_r-lag Type
Achievement of ZVS for leading switches	Filter inductor provides the energy $\frac{1}{2}(K^2L_f)I_p^2(t_1)$	Filter induction and resonant inductor provides the energy $\frac{1}{2}(K^2L_f+L_r)I_p^2(t_1)$
Achievement of ZVS for lagging switches	$\frac{1}{2}L_rI_p^2(t_1)$	$\frac{1}{2}L_rI_p^2(t_3)$
The conduction times of clamping diodes in a switching cycle	Twice	Once
Conduction loss at zero state	Be proportional to the square of $I_p(t_1)$	Be proportional to the square of $I_p(t_3)$
Duty cycle loss	$D_{loss}=\frac{t_{36}}{T_s/2}=\frac{4L_r\cdot[I_p(t_1)+I_p(t_6)]}{V_{in}\cdot T_s}$	$D_{loss}=\frac{t_{36}}{T_s/2}=\frac{4L_r\cdot[I_p(t_3)+I_p(t_6)]}{V_{in}\cdot T_s}$

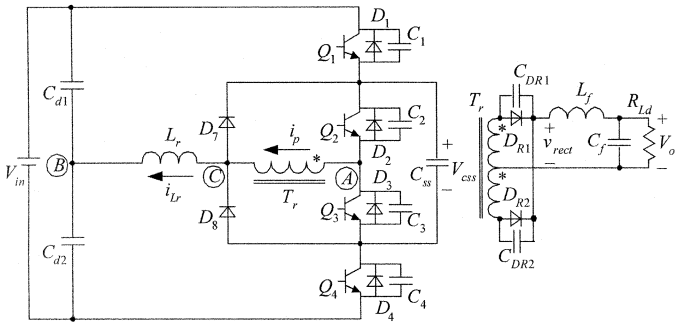

Fig. 5. Simplified improved ZVS PWM TL converter.

large enough to be treated as a voltage source with value $V_{in}/2$ at steady state, during $[t_1, t_4]$ the primary current i_p could flow through another path, i.e., the lower voltage source $V_{in}/2$, $Q_4(D_4)$ and C_{ss}, where v_{AB} is also zero. And during $[t_4, t_5]$, i_p could flow through another path, i.e., the lower voltage source $V_{in}/2$, $Q_4(D_4)$ and $Q_3(D_3)$, where v_{AB} also equals $-V_{in}/2$. Therefore D_5 could be removed. Similarly, D_6 could be removed. Thus, the proposed ZVS PWM TL converter in Fig. 2 can be simplified as Fig. 5. Fig. 6 gives the equivalent circuits of four switching modes corresponding to Fig. 3(c)-(f).

VI. THE EFFECT OF THE BLOCKING CAPACITOR

In practical circuit, there is slight difference between drive signals of two pairs of switches resulted by the control circuit and/or drive circuits. Also the two pairs of switches are not so matched. Therefore, there is slight difference between the conducting time of the four switches, which results in saturating of transformer. A blocking capacitor C_b is usually introduced to the primary side to prevent the transformer from saturating. The blocking capacitor can be in series with T_r or L_r. Therefore, there are four different topologies of ZVS PWM TL converter, which are shown in Fig. 7.

In T_r-lead type converter, the clamping diodes conduct twice in a switching cycle. One occurs in zero state, both the transformer and the resonant inductance are shorted. The other occurs after the output rectified voltage is clamped, the resonant inductance is shorted. If C_b is in series with the resonant inductance, the dc component across it will result in asymmetry of the resonant inductance current in positive and negative direction when the resonant inductance (including C_b) is shorted (see Fig. 8); If C_b is in series with the transformer, the dc component across it will result in asymmetry of the primary current in positive and negative direction when the transformer is shorted (including C_b) (see Fig. 9). The asymmetry of i_p or i_{Lr} will result in asymmetry between the currents of two clamping diodes.

In T_r-lag type converter, the clamping diodes only conduct after the rectified voltage is clamped. At that time, only the resonant inductance is shorted. If C_b is in series with the resonant inductance, the dc component across it will result in asymmetry of the resonant inductance current when the resonant inductance (including C_b) is shorted (see Fig. 10); If C_b is in series with the transformer, the dc component across it will not result in asymmetry of the primary current, because that the transformer is not shorted by the clamping diodes.

Therefore, the best scheme of the four converters is to insert the blocking capacitor into the T_r-lag Type converter and it is in series with the transformer, as shown in Fig. 7(d).

VII. DESIGN PROCEDURE

This section illustrates a simplified design procedure and example. The design of this converter involves complex interactions between circuit parameters and operation condition. Therefore we should make some assumptions and approximations.

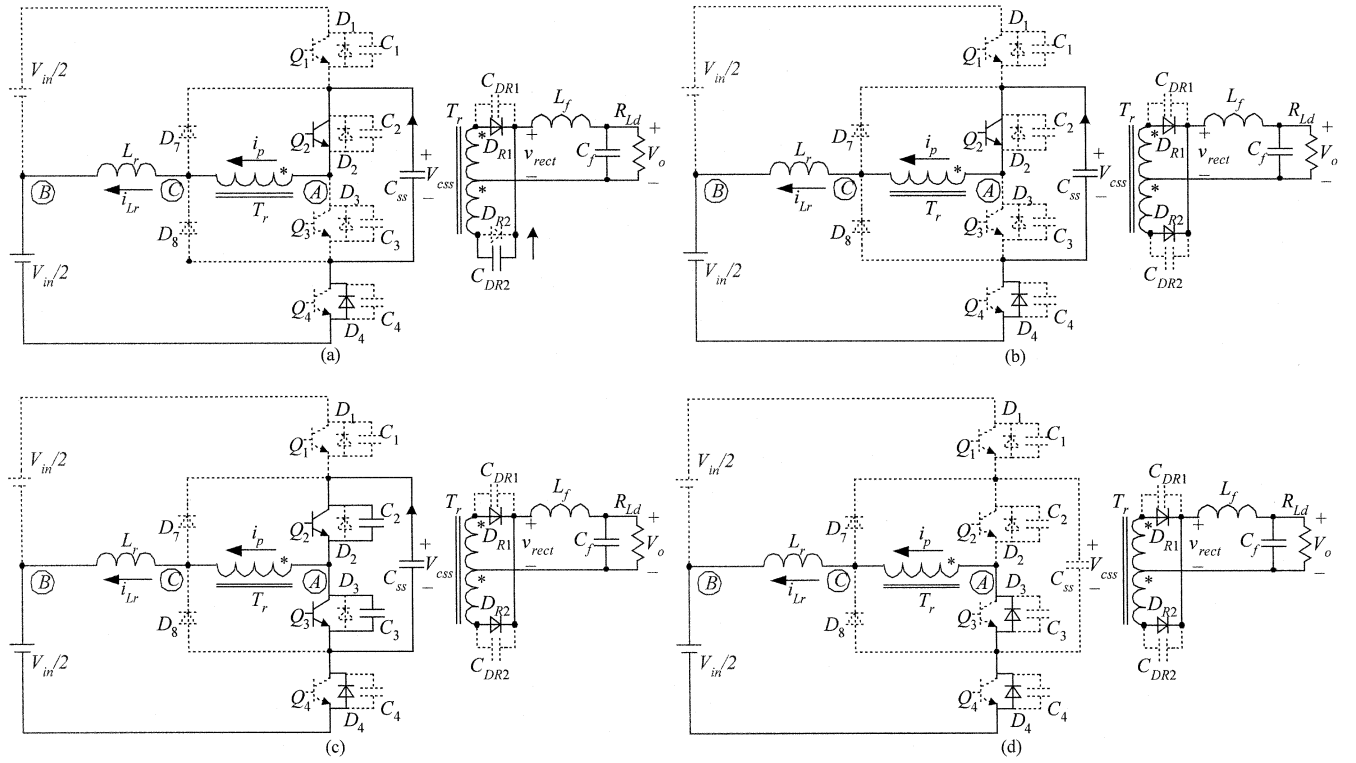

Fig. 6. Equivalent circuits of four switching modes of the simplified converter. (a) $[t_1, t_2]$. (b) $[t_2, t_3]$. (c) $[t_3, t_4]$. (d) $[t_4, t_5]$.

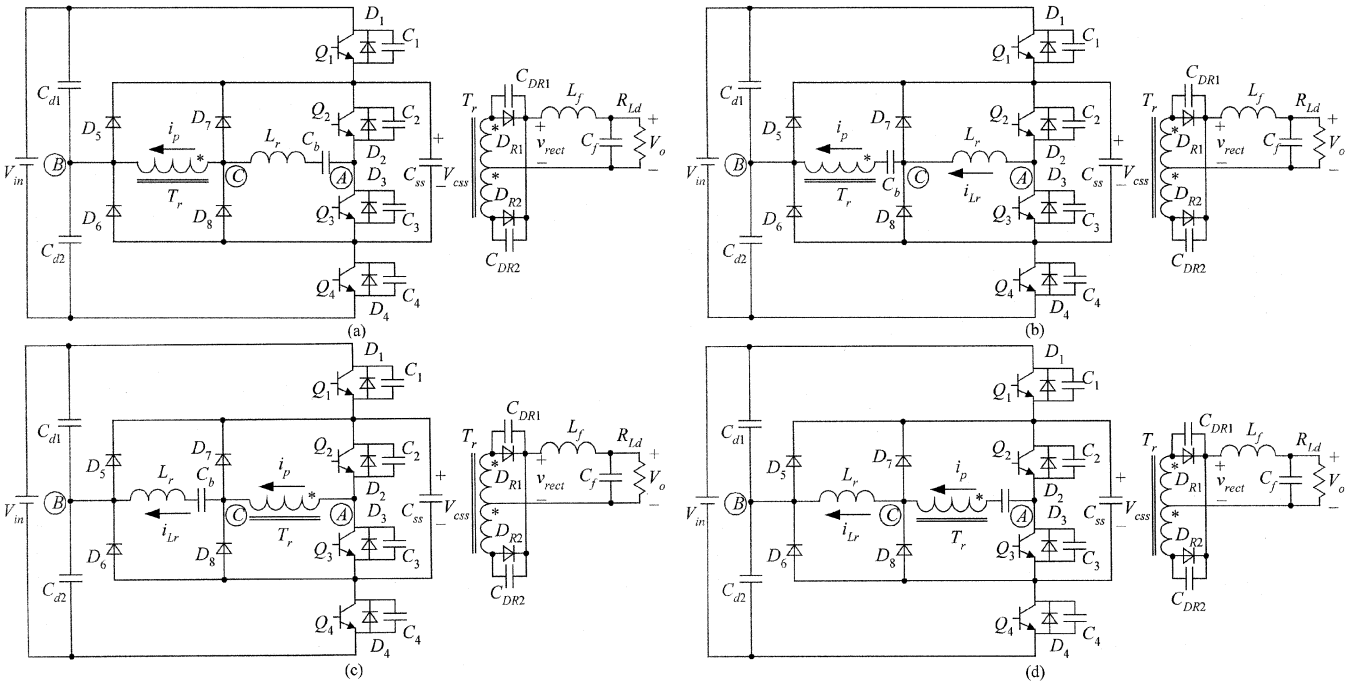

Fig. 7. Four topologies. (a) T_r-lead-*LC* Type. (b) T_r-lead-*TC* Type. (c) T_r-lag-*LC* Type. (d) T_r-lag-*TC* Type.

1) The input specifications:
Input voltage: $V_{in} = 540$ VDC $\pm 20\%$;
Output voltage: $V_o = 250$ VDC;
Output current: $I_o = 10$ A;
Switching frequency: $f_s = 50$ kHz; Switching period: $T_s = 20$ μs.

2) Let $D_{\text{eff max}} = 0.8$ at the lowest input voltage, then the turns ratio of the transformer K is determined by the following equation:

$$K = \frac{\frac{V_{\text{in min}}}{2}}{\frac{(V_o + V_D)}{D_{\text{eff max}}}} = 0.687 \tag{21}$$

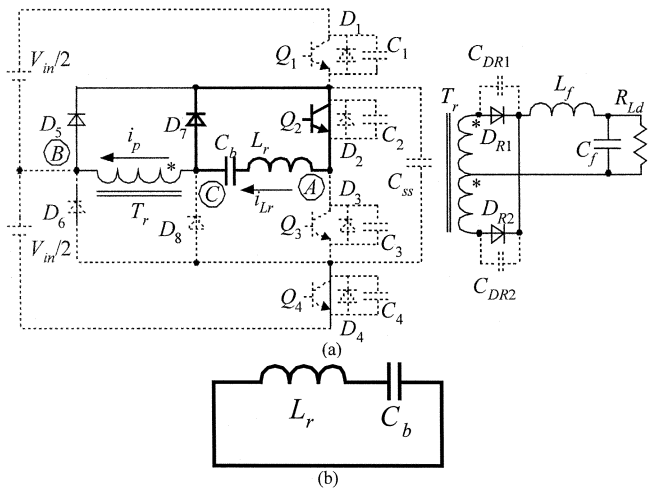

Fig. 8. Equivalent circuit of T_r-lead-*LC* Type when the clamping diodes conduct. (a) Equivalent circuit. (b) Further equivalent circuit.

where V_D is the voltage drop in the secondary rectifier diode and $V_D = 1.5$ V.

The number of turns of the primary and secondary winding are selected at 11 and 16, respectively, thus, $K = 0.688$.

3) Let the maximum duty cycle loss $D_{\text{loss max}} = 0.1$, $I_p(t_3)$ can be calculated by (1)–(6), and $I_p(t_6)$ is I_o/K approximately. According to (20), L_r can be calculated as

$$L_r = \frac{D_{\text{loss max}} \cdot V_{in\,\min} \cdot T_s}{4[I_p(t_3) + I_p(t_6)]} = 8.2\ \mu\text{H}. \tag{22}$$

A value equal to 8 μH is adopted, then $D_{\text{loss max}} = 0.108$, and the maximum primary duty cycle $D_{pmax} = D_{\text{eff max}} + D_{\text{loss max}} = 0.8 + 0.108 = 0.908 < 1$, so $L_r = 8\ \mu$H is reasonable.

4) The chosen MOSFET ($2 * \text{IRF460A}$) to meet the voltage and current requirements has an intrinsic capacitor $C_{oss} = 2 * 130$ pF.

According to (19), the minimum current to ensure ZVS for the lagging switch is

$$I_{lag\_\min} = \frac{V_{in}}{2} \cdot \sqrt{\frac{8}{3} \cdot \frac{C_{oss}}{L_r}} = \frac{540}{2} \cdot \sqrt{\frac{8}{3} \cdot \frac{2 \times 130 \times 10^{-12}}{8 \times 10^{-6}}} = 2.5\ \text{A} \tag{23}$$

which corresponds to $2.5 \times 0.688 = 1.7$ A load current, representing 17% of the full load.

The delay time of the gate drives of the leading switches is set as $t_{d(\text{lead})} = 300$ ns. The current for the output capacitor of the in-coming switch to be fully discharged during the delay time is

$$I_1 = \frac{V_{in}}{2t_{d(\text{lead})}} \cdot (2C_{\text{lead}} + C'_D). \tag{24}$$

It is very difficult to obtain the value of C'_D. From the experimental results, we can know that about 4/5 of the reflected output current is used to charge/discharge the output capacitors

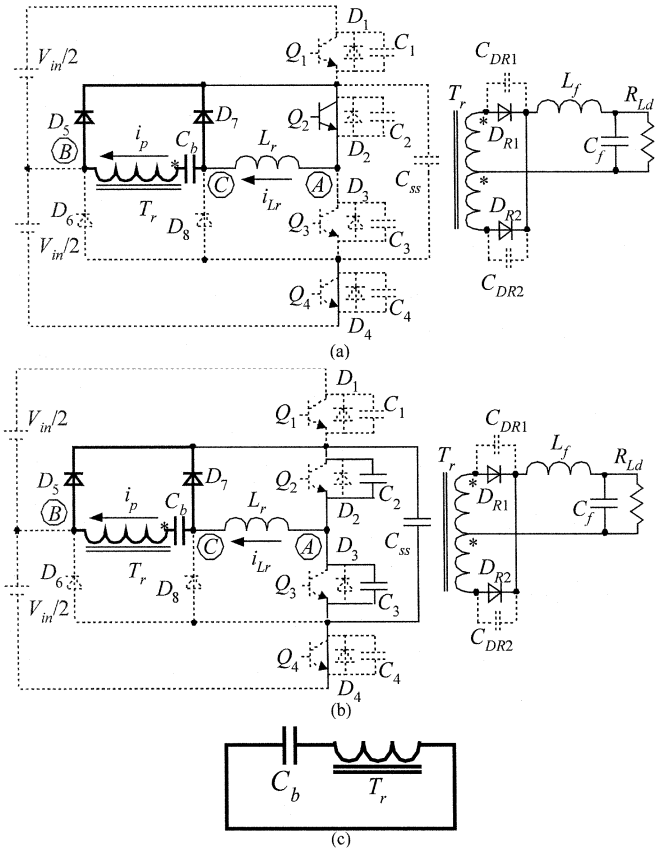

Fig. 9. Equivalent circuit of T_r-lead-*TC* Type when the clamping diodes conduct. (a) Equivalent circuit 1. (b) Equivalent circuit 2. (c) Further equivalent circuit.

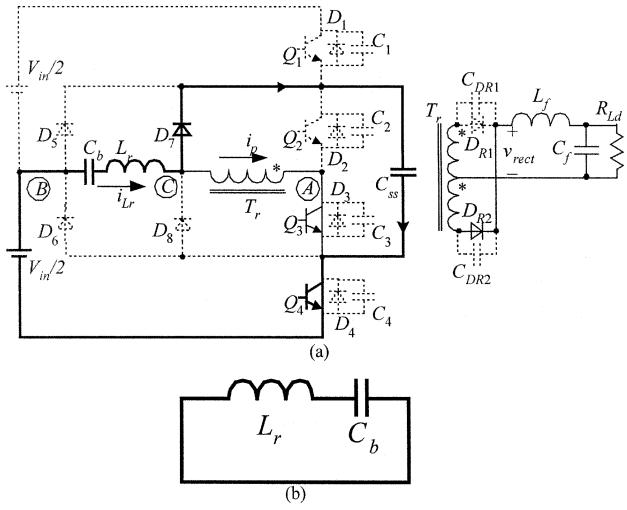

Fig. 10. Equivalent circuit of T_r-lag-*LC* Type when the clamping diodes conduct. (a) Equivalent circuit. (b) Further equivalent circuit.

of the leading switches, and $C_{\text{lead}} = (4/3)C_{oss}$, so (24) could be approximately simplified to

$$\frac{4}{5}I_1 = \frac{V_{in}}{2t_{d(\text{lead})}} \cdot 2 \cdot \frac{4}{3}C_{oss} \tag{25}$$

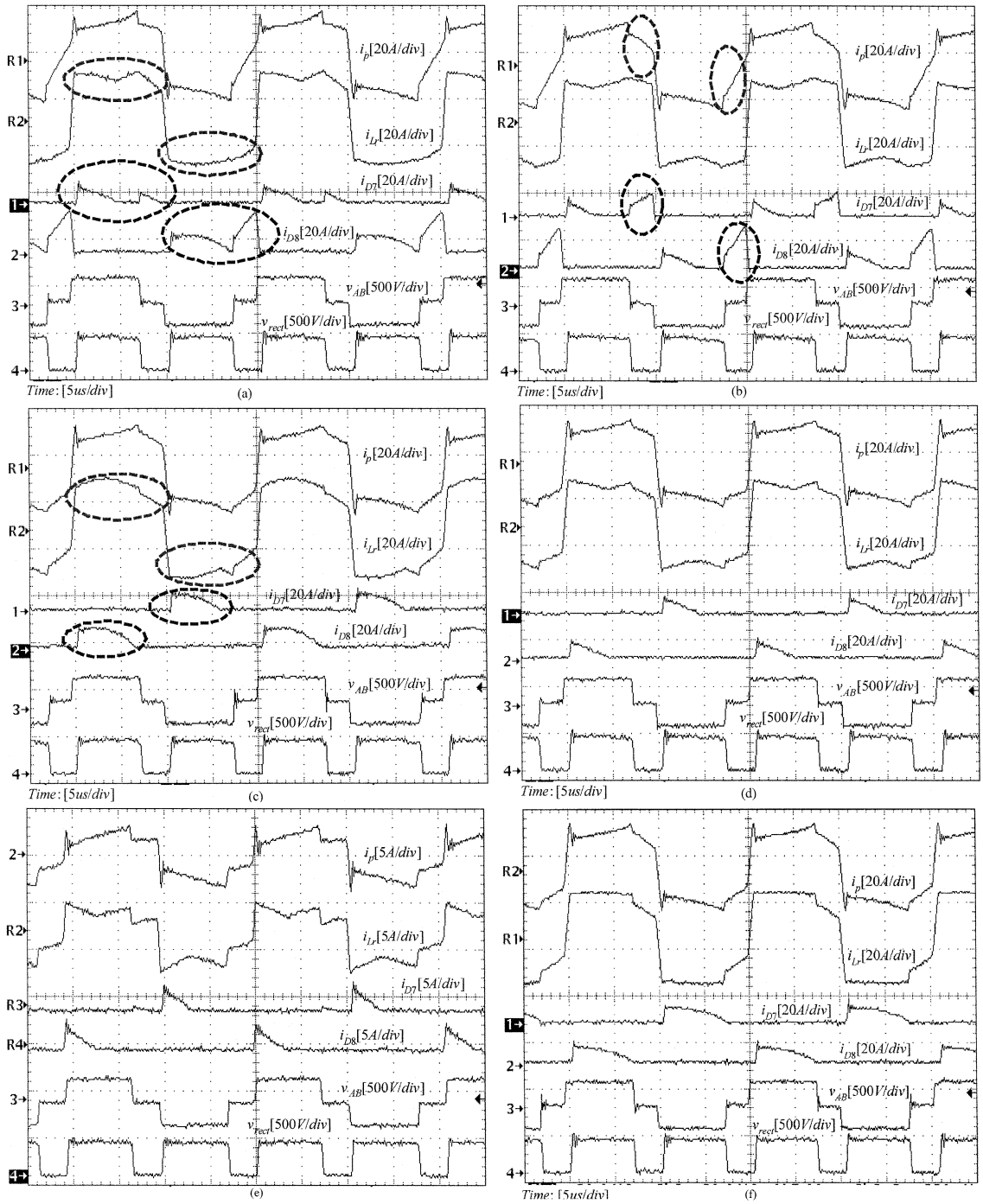

Fig. 11. Experimental waveforms. (a) T_r-lead-*LC* Type. (b) T_r-lead-*TC* Type. (c) T_r-lag-*LC* Type. (d) T_r-lag-*TC* Type. (e) The waveforms of T_r-lag-*TC* Type under 10% load. (f) The waveforms of simplified T_r-lag-*TC* Type.

$$\text{Then } I_1 = \frac{V_{in}}{t_{d(\text{lead})}} \cdot \frac{5}{3} C_{oss} = \frac{540}{300 \times 10^{-9}} \cdot \frac{5}{3} \cdot 2 \times 130 \times 10^{-12} = 0.78 \text{ A} \quad (26)$$

which corresponds to $0.78 \times 0.688 = 0.54$ A load current, representing 5.4% of the full load. It is coincident with the Section III, where we got the conclusion that the leading switches could realize ZVS at light load.

VIII. Experimental Results

A 2.5-kW prototype converter was built in our lab to verify the four topologies of the ZVS PWM TL converter and the simplified converter. The universal PS PWM control is applied, which is proposed in [3], and UC3895 is employed as a core control IC. The specifications of the prototype are as follows: Input voltage: $V_{in} = 540$ VDC $\pm$ 20%; Output voltage: $V_o = 250$ VDC; Output current: $I_o = 10$ A; $Q_1(D_1$ and $C_1)$–$Q_4(D_4$ and $C_4)$: IRF460 $*$ 2; D_5 – D_8: DSEI30-06A; D_{R1} – D_{R2}: DSEI30-10A; Blocking capacitor:

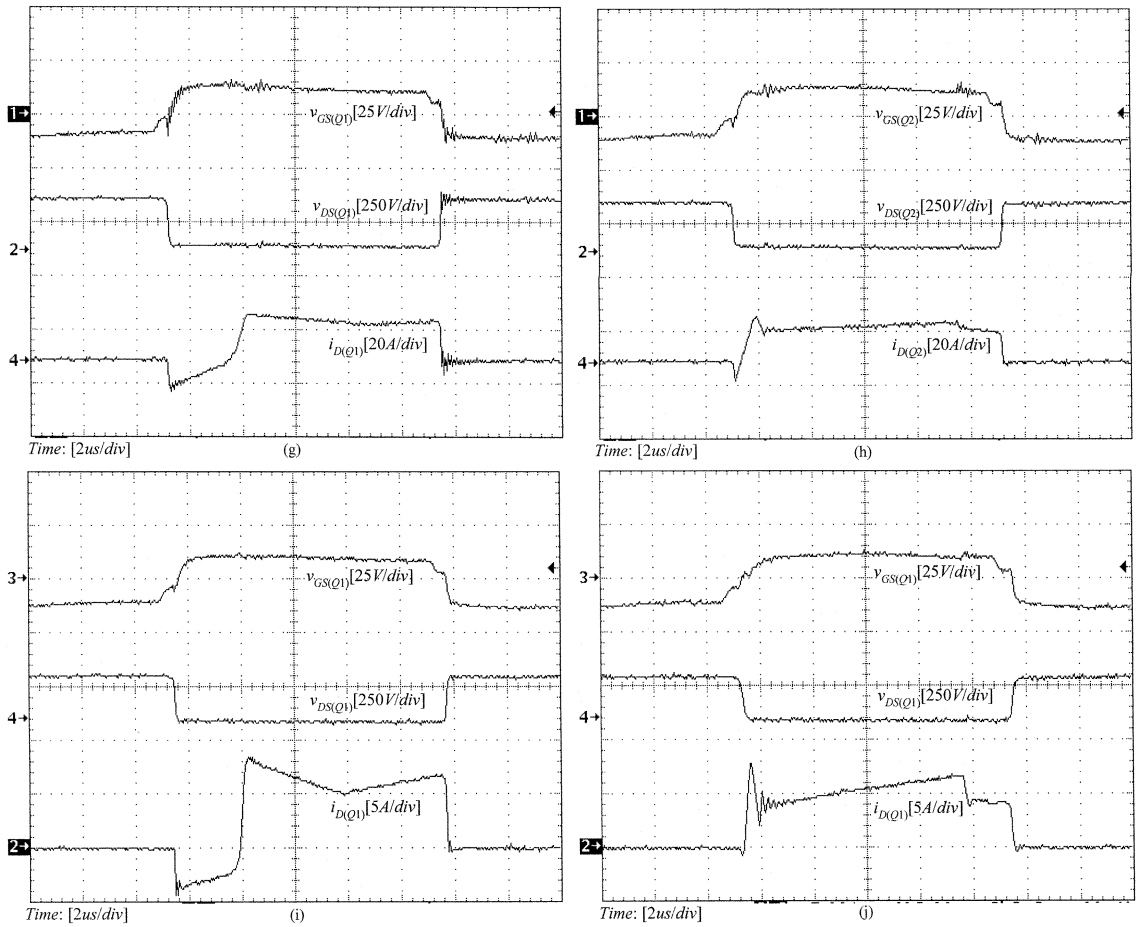

Fig. 11. (*Continued.*) Experimental waveforms. (g) v_{GS}, v_{DS}, and i_D of the leading switch Q_1 under full load. (h) v_{GS}, v_{DS}, and i_D of the lagging switch Q_2 under full load. (i) v_{GS}, v_{DS}, and i_D of the leading switch Q_1 under 20% full load. (j) v_{GS}, v_{DS}, and i_D of the lagging switch Q_2 under 20% full load.

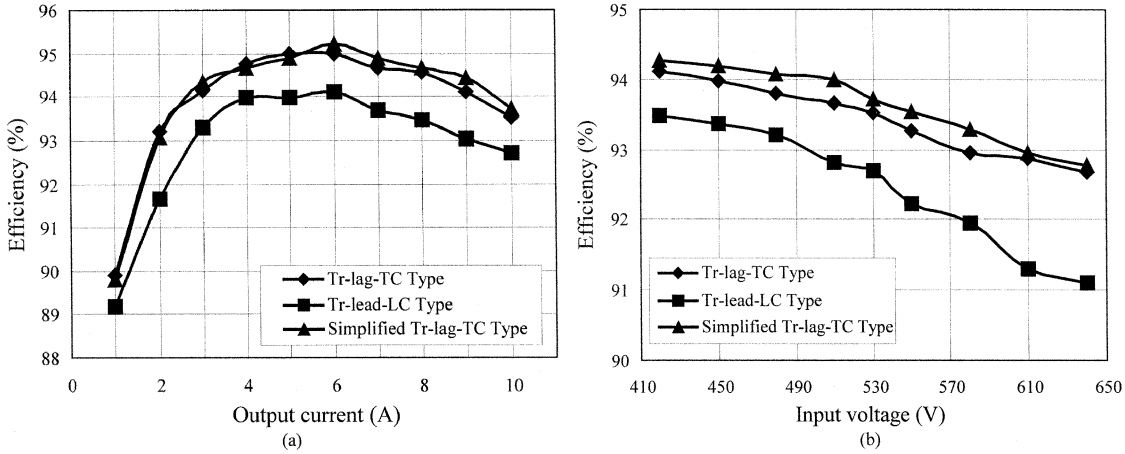

Fig. 12. The overall efficiency. (a) Efficiency at different output current under the normal input voltage. (b) Efficiency at full load under different input voltage.

$C_b = 5\ \mu$F; Transformer turns ratio: $K = 0.688$; Output filter inductor: $L_f = 480\ \mu$H; Switching frequency: $f_s = 50$ kHz.

Fig. 11(a)–(d) shows the waveforms i_p, i_{Lr}, i_{D7}, i_{D8}, v_{AB}, and $v_{\rm rect}$ of four different topologies at full load. It can be seen that $v_{\rm rect}$ has no oscillation and no voltage spike. They also illustrate that D_7 and D_8 of T_r-lead Type conduct twice in one switching cycle, however, that of T_r-lag Type conduct only once. At zero state, i_{Lr} of T_r-lag Type is less than that of T_r-lead Type, which results in reducing switching loss and increasing efficiency.

As shown in Fig. 11(a) and (c), when the blocking capacitor C_b is in series with the resonant inductance, the dc component across it results in asymmetry of the resonant inductance current, and as a result, the currents of the two clamping diodes are asymmetrical. Fig. 11(b) illustrates that when C_b is in series with the transformer in T_r-lead type converter, the primary current is asymmetric, and the currents of the two clamping diodes are asymmetrical accordingly. Fig. 11(d) indicates that when C_b is in series with the transformer in T_r-lag type converter, the transformer current is symmetrical, and the currents of the

two clamping diodes are symmetrical accordingly. As Fig. 11 clearly illustrates, the converter in Fig. 7(d) is the best scheme.

Fig. 11(e) shows the waveforms of T_r-lag-*TC* Type under 10% load., which means that the converter operates well under low load. It also shows the stability of the improved topology at the variable load conditions.

Fig. 11(f) shows i_p, i_{Lr}, i_{D7}, i_{D8}, v_{AB}, and $v_{\rm rect}$ of the simplified converter of T_r-lag-*TC* Type, $v_{\rm rect}$ also has no oscillation and no voltage spike, which thanks to the two clamping diodes. Clamping diode work not only as a clamping diode, but also as a freewheeling diode.

Fig. 11(g) gives the gate drive signal v_{GS}, the voltage across the drain and source v_{DS} and the drain current i_D of the leading switch Q_1 under full load, which illustrates that Q_1 is zero-voltage turn-off thanks to C_1 and C_4, and before Q_1 turns on, $v_{DS(Q1)}$ reduces to zero and clamped by the anti-paralleled diode of Q_1 and C_{ss}, so Q_1 is zero-voltage turn-on. Fig. 11(h) gives v_{GS}, v_{DS}, and i_D of the lagging switch Q_2, which illustrates that Q_2 is zero-voltage turn-off thanks to C_2 and C_3, and before Q_2 turns on, its anti-paralleled diode conducts and clamps $v_{DS(Q2)}$ at zero, so Q_2 is zero-voltage turn-on.

Fig. 11(i) and (j) gives v_{GS}, v_{DS}, and i_D of Q_1 and Q_2 under 20% full load, respectively. From the figures, it can be seen that Q_1 and Q_2 still realize ZVS, and the experimental results are well in agreement with the theoretical analysis.

Fig. 12 gives the conversion efficiency of the three kinds of ZVS PWM TL converters: 1) T_r-lead-*LC* Type converter; 2) T_r-lag-*TC* Type converter; 3) the simplified T_r-lag-*TC* Type converter. Fig. 11(a) shows the efficiency at different output current under the nominal input voltage. The efficiency of T_r-lag Type-*TC* converter under full load is about 93.5%. Fig. 11(b) shows the efficiency at full load under different input voltage.

From Fig. 12, we can seen that the efficiency of T_r-lag-*TC* Type converter and the simplified converter are nearly the same, the reason is that during $[t_1, t_5]$ the resonant inductor current flows through two paths in T_r-lag-*TC* Type, one is through the clamping diode and the other is through the freewheeling diode. As for the simplified converter, the current also flows through two paths, one through the clamping diode, the other through $V_{in}/2$, $Q_4(D_4)$, or $Q_1(D_1)$ and C_{ss}. Although the flowing paths are different, the sum of conduction losses in the two paths is nearly the same during $[t_1, t_5]$ because the current of the resonant inductor is the same in both the converters.

IX. Conclusion

This paper proposes an improved ZVS PWM TL converter, which is an improvement from the original one by exchanging the position of the resonant inductor and the transformer. The improved converter has several advantages over the original as follows:

1) the clamping diode conducts only once, and the current rating of clamping diode is less;
2) the conducting loss at zero state is less, and efficiency can be increased;
3) the duty cycle loss is less.

This paper also analyzes the effects of the blocking capacitor in different positions and a best scheme is determined. The theoretical analysis is verified by experimental results.

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