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A 50–60 V Class Ultralow Specific on-Resistance Trench Power MOSFET *

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A 50–60 V class ultralow specific on-resistance ($R_{on,sp}$) trench power MOSFET is proposed. The structure is characterized by an n^+-layer which is buried on the top surface of the p-substrate and connected to the drain n^+-region. The low-resistance n^+-layer shortens the motion-path in high-resistance n^- drift region for the carriers, and therefore, reduces the $R_{on,sp}$ in the on-state. Electrical characteristics for the proposed power MOSFET are analyzed and discussed. The 50–60 V class breakdown voltages (V_B) with $R_{on,sp}$ less than 0.35 mΩ·cm^2 are obtained. Compared with several power MOSFETs, the proposed power MOSFET has a significantly optimized dependence of $R_{on,sp}$ on V_B.

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Because of its ease of integration, power metal oxide semiconductor field effect transistors (MOSFETs) have been key components in power integrated circuits used in portable power management products. The long drift region in conventional lateral power MOSFETs limits the improvements of the specific on-resistance ($R_{on,sp}$), which results in a contradiction between the breakdown voltage V_B and the $R_{on,sp}$. Power MOSFETs with trench-based technology have been shown to reduce $R_{on,sp}$ because of the reduced cell pitch, and therefore, is attracting increasing attention.[1−3] Fujishima and Salama proposed a trench lateral power MOSFET with a trench bottom drain contact with the simulated performances of $V_B = 80$ V and $R_{on,sp} = 0.8$ mΩ·cm^2.[4] In 2007, Varadarajan *et al.*[5] introduced trench-gate into the conventional trench MOSFET and proposed a double-trench power MOSFET, which exhibited an $R_{on,sp}$ of 7 mΩ·cm^2 with a V_B of 250 V, and almost meanwhile, 80 V class double-trench MOSFETs with a planar drain or a plug drain were studied by them.[6−8] In 2011, Luo *et al.*[9] introduced trench power MOSFETs into silicon-on-insulator substrates. Based on the previous investigation on high voltage power devices,[10−13] in this Letter a novel 50–60 V class trench power MOSFET with an ultralow $R_{on,sp}$ is investigated. The mechanism of the proposed MOSFET is discussed. Electrical characteristics for the device are analyzed and compared with several existing structures.

The proposed power MOSFET is shown in Fig. 1. There are two trenches in the device: an oxide-filled trench supporting almost all the lateral voltage whose length defines the drift region length, and a polysilicon-filled trench etched into the p-well to the n^- silicon layer which provides a vertical channel in the on-state. The most important characteristic of the MOSFET is the n^+-layer buried on the top surface of the p-substrate which is connected to the drain n^+-region. For the conventional trench MOSFET in the on-state,[5] the carriers flow along the lowly doped silicon (high-resistance) all around the trench. However, for the proposed structure as shown in Fig. 1, the lowly doped silicon is only under the source side because of the n^+-layer (low-resistance) buried on the interface. That is to say, the motion-path of the carriers in the high-resistance silicon is shortened, and therefore, the $R_{on,sp}$ of the device is reduced. Only an additional process of n^+-layer implantation is needed to form the proposed structure and the other fabrication processes are fully compatible with conventional trench technology. The proposed power MOSFET is simulated using the two-dimensional device simulator MEDICI.[14] The structural parameters are shown in Table 1.

In the off-state (a positive voltage V_{ds} is applied to the drain while the source, gate and substrate are grounded), V_B of the MOSFET device is determined by the smaller value of vertical V_B ($V_{B,V}$) and lateral V_B ($V_{B,L}$). Figure 2(a) shows the equipotential contours at breakdown for the proposed power MOSFET with the structural parameters of $W_t = 0.5$ μm, $H_t = 5$ μm, and $N_n = 2 \times 10^{15}$ cm^{-3}. It can be seen that $V_{B,V}$ is supported by a vertical n^+p^- parallel plane junction (consisting of interface n^+-layer and p^--substrate layer) just as the V_1 shown in Fig. 2(a). Figure 2(b) shows the vertical electric field distributions with different N_{sub}: the maximum electric fields become smaller with the decreasing N_{sub}. However, the widths of depletion regions in the p^- substrate are extended, which lead to a $V_{B,V}$ having nothing to do with N_{sub}. $V_{B,L}$ is determined by the relationship of $V_{B,L} = \min(V_2, V_3)$. Here V_2 is supported by a p–n junction (consisting of p-well region and n^- drift region) which is mainly affected by the N_n and H_t, and V_3 is supported by the oxide-filled trench which is mainly affected by the W_t as shown in Fig. 2(a). Figure 2(c) shows the dependences of V_B on W_t and H_t. It can be seen that 50–60 V class breakdown voltages are obtained for the proposed power MOSFET. When H_t is one fixed value in the range of 3–6 μm, V_B increases

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with the increasing W_t because of a higher V_3. When W_t is one fixed value from 0.3 to 0.7 μm, V_B is firstly enhanced with an increased H_t (V_2 is enhanced), and finally reaches a saturation value resulting in a saturating V_3. V_B with a W_t of 0.3 μm is a straight line because V_B is always determined by V_3, which is irrelevant to H_t in the condition of $W_t = 0.3$ μm.

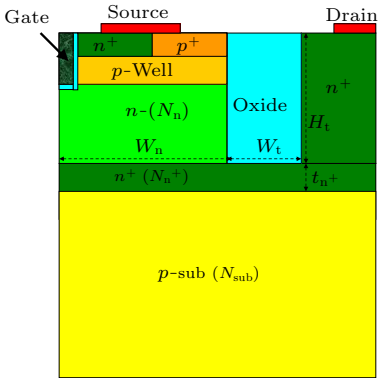

Fig. 1. Cross section of the proposed power MOSFET.

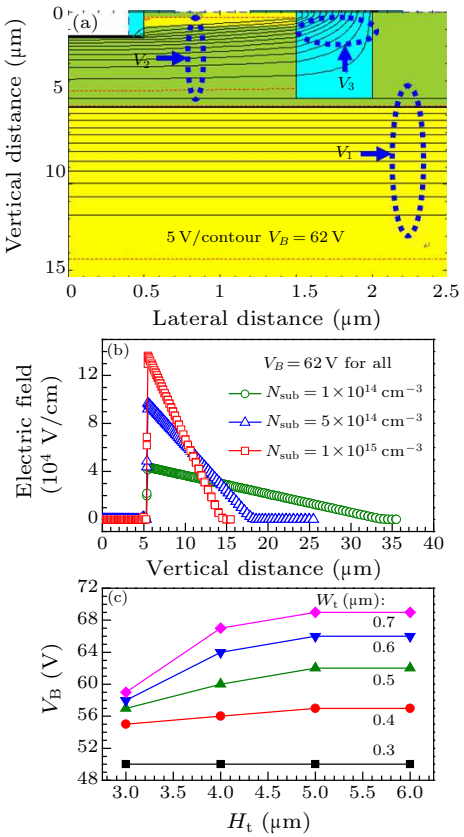

Fig. 2. Off-state characteristics of the proposed power MOSFET. (a) The equipotential contours distribution at breakdown for $W_t = 0.5$ μm, $H_t = 5$ μm, $N_n = 2 \times 10^{15}$ cm^{-3} and $N_{sub} = 1 \times 10^{15}$ cm^{-3}. (b) Dependences of V_B on N_{sub} for $W_t = 0.5$ μm, $H_t = 5$ μm, and $N_n = 2 \times 10^{15}$ cm^{-3}. (c) Dependences of V_B on W_t and H_t.

In the on-state (a positive voltage V_{ds} and V_{gs} are applied to the drain and gate, respectively, while the source and substrate are grounded), the introduced interface buried n$^+$-layer (low-resistance) shortens the distance between the channel and n$^+$ region at drain side compared with the conventional trench MOSFET, which will lead to a lower $R_{on,sp}$ just as shown in Fig. 3(a) (an ultralow $R_{on,sp}$ of 0.17 mΩ·cm^2 is obtained). Figure 3(b) is the dependences of $R_{on,sp}$ on W_t and H_t. It can bee seen that $R_{on,sp}$ becomes larger with the increasing W_t and H_t: the increasing W_t leads to an increased device pitch cell, and the increasing of H_t leads to an increasing height of low-resistance n$^-$ drift region. For the proposed 50–60 V class power MOSFET, $R_{on,sp}$ less than 0.35 mΩ·cm^2 is always got. $R_{on,sp}$ versus V_B for several power MOSFETs is compared with as shown in Fig. 4. A significantly optimized dependence of $R_{on,sp}$ on V_B is obtained for the proposed power MOSFET in the voltage range of 50–70 V. Because of the electronic potential flows only toward to the source side as shown in Fig. 2(a), the V_B of the proposed structure is lower than the conventional trench MOSFET with the same dimensions of the oxide-filled trench.

Table 1. Device parameters used in the simulation.

Parameter	Value
Length of n$^-$ drift region, W_n (μm)	1.5
Length of oxide-filled trench, W_t (μm)	0.3–0.7
Thickness of oxide-filled trench, H_t (μm)	3–6
Thickness of n$^+$ layer on the interface, t_{n+} (μm)	0.5
Concentration of n$^-$ drift region, N_n (cm^{-3})	Need to be optimized
Concentration of p$^-$substrate, N_{sub} (cm^{-3})	(0.1–1) × 10^{15}
Concentration of interface n$^+$-layer, N_{n+} (cm^{-3})	1 × 10^{19}

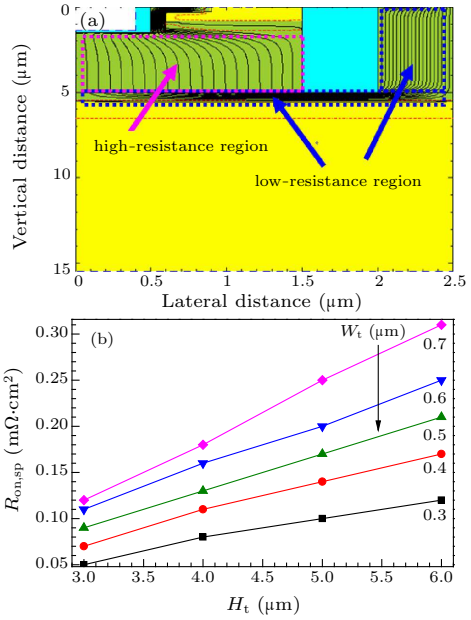

Fig. 3. On-state characteristics of the proposed power MOSFET. (a) The current flowfine contours at $V_{gs} = 15$ V and $V_{ds} = 0.25$ V with the structure parameters of $W_t = 0.5$ μm, $H_t = 5$ μm, and $N_n = 2.0 \times 10^{15}$ cm^{-3}. (b) Dependences of $R_{on,sp}$ on W_t and H_t.

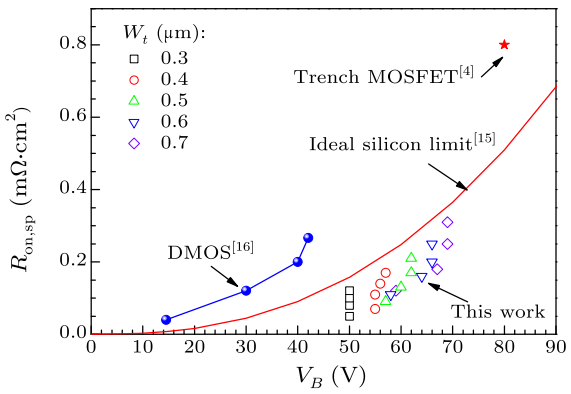

Fig. 4. Dependences of $R_{on,sp}$ on V_B for several power MOSFETs. $R_{on,sp}$ is calculated without electrode area for all.

A novel trench power MOSFET is investigated. The low-resistance n^+-layer buried on the interface in the proposed power MOSFET shortens the motion-path in the high-resistance n^- drift region for the carriers in the on-state, and therefore, reduces the $R_{on,sp}$. 50–60 V class V_B with $R_{on,sp}$ less than 0.35 mΩ·cm^2 is obtained for the proposed power MOSFET.

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