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Abrasive electrochemical multi-wire slicing of solar silicon ingots into wafers

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ABSTRACT

To meet the growing demands of the global photovoltaic (PV) industry, preparing large scale and ultrathin solar wafers becomes one of the key issues. This paper presents the preparatory investigations of slicing solar silicon ingot into wafers by an abrasive electrochemical method based on a multi-wire saw system. The anodic passivation on silicon can be controlled by applying an anodic potential during the mechanical slicing process, which improves the surface integrity and material removal rate remarkably. This new hybrid machining method has no influence on subsequent cleaning of wafers and preparing the solar cells, and the average photoelectric transformation efficiency is >17.5%.

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1. Introduction

Multi-wire sawing is the main slicing technique of the photovoltaic industry currently [1], which allows for a high throughput, a small kerf loss and a good surface quality, enabling the wafers to be used without any further machining. The current state of the art is to produce solar cell wafers 156 mm \times 156 mm as thin as 200 μ m or less [2]. However, the roadmap of the PV-industry points towards the next generation of 210 mm \times 210 mm and larger whilst reducing the thickness even further down to 100 μ m. Meanwhile, the goal is to reduce the kerf loss as well as increasing the cutting rate. Since the method of multi-wire sawing uses contact force to perform its cut-grinding process that easily results in harmful surface micro-cracks or other damage to the wafer. Basic knowledge about the microscopic details of the sawing process is required and is subject to ongoing research.

Wire electrical discharge machining (WEDM) is a new potential technique for silicon slicing [3]. In this method, silicon is eroded by electric sparks and sliced by thermal dissolution. Peng and Liao [4] and Okada et al. [5] reported that since the wire was not in contact with the silicon ingot, it was possible to reduce the wafer thickness and decrease the kerf loss below that of traditional sawing methods. Recently, the possibility of slicing silicon ingots by wire electrolytic-spark hybrid machining is also discussed [6], in which heat affected zone and harmful metal residues are considerably diminished. Unfortunately, efficiency is of the utmost importance. These new methods can only slice several pieces of wafers simultaneously and cannot be easily introduced into a multi-wire sawing system due to the processing incompatibility.

In this paper, the improvement of slicing the solar silicon ingot into wafers is investigated by using an abrasive electrochemical method based on a multi-wire saw system. This new approach has no influence on subsequent cleaning of wafers and preparing the

* Corresponding author. E-mail address: wangwei@nuaa.edu.cn (W. Wang). solar cells, and the average photoelectric transformation efficiency is $>\!17.5\%$

2. Experimental procedure

In an attempt to explore the abrasive electrochemical multiwire slicing technique, some improvements inclusive of DC power supply and electrical connecting method have been adopted in a multi-wire saw system, which are necessary to this new kind of hybrid machining.

Then the silicon ingots are sliced into wafers. After these wafers have been separated, they are washed and the dimensions are measured, as shown in Fig. 1.

After that, these wafers are forwarded the next photolithographic, doping and contacting processing for the final photoelectric transformation efficiency test. In comparison to abrasive electrochemical multi-wire sawing, the same silicon material is sliced by traditional multi-wire saw methods.

2.1. Equipment

The abrasive electrochemical multi-wire saw schematics are shown in Fig. 2(a). In comparison to the traditional multi-wire saw system, DC power supply is the only distinct difference between them.

A single wire, served as the cathode, with a typical diameter of 120–140 μ m and a spool length of 600–800 km, is fed from the supply spool through a wire tensioning system to the wire guide rollers, which are grooved with a constant pitch. By winding the wire over these wire guide rollers (WGR) a wire web is formed. On the output end, a take-up spool collects the used wire. The abrasive slurry, supplied through a system of nozzles onto the wire web, is carried with the moving wire into the sawing channel where it performs its cut-grinding process. This slurry consists of hard grinding particles, generally SiC with a grain size in the range of 10–15 μ m that are suspended in the electrolyte (Polyethylene glycol, i.e., PEG, the electric conductivity is from 100 μ s/cm to

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Fig. 1. Experimental steps for manufacturing of the wafers.

 $500 \ \mu$ s/cm). By pushing the silicon workpieces (the anode) against the wire web they are sliced into thousands of wafers in one single run. Here NTC 442D (NTC, Japan) has been selected to be the experimental system as shown in Fig. 2(b).

2.2. Experimental conditions

As can be seen from Table 1, the main characteristic of this new slicing method is the use of the anodic passivation. The corrosion potential is ranging from 5 V to 20 V. As one of the crucial parameters, the electrical parameters for this process are important, so, a high resolution and high speed programmable DC power supply has been introduced. The main characteristics are low ripple and noise, very high accuracy and resolution of 0.1 mV/0.1 mA.

Generally, silicon ingot has been glued on the glass plate mounted on the fixtures, which are isolated from the machine body. In order to keep the silicon ingot as the anode, it has to be connected with the DC power supply. Due to the different characteristics of silicon ingot compared to metals of good conductance, especially for the metal semiconductor barrier, we cannot use metal materials as a conductive layer. What's more, the wire could be broken because of it. So the electrical connecting method needs to be reconsidered. The feasible approach is to use conductive adhesive between the glass plate and silicon ingot.



Fig. 2. (a) The abrasive electrochemical multi-wire saw schematics, and (b) experimental saw system, silicon ingots mounted on the fixtures.

Table 1 Experimental conditions.	
Abrasive electrochemical multi-wire sawing	
$\label{eq:ansatz} \begin{array}{l} \mbox{Material(anode): mono p-type Si(1.6-1.8 Ω cm)} \\ \mbox{Wire(cathode): Stainless steel($00.12 mm$)(Cu coated)} \\ \mbox{Coolant: PEG(150-200 μs/cm)} \\ \mbox{Slurry: SiC} \\ \mbox{Voltage: 5-20V} \\ \mbox{Wire speed: about 600 m/min} \\ \mbox{Feed rate: } 0.45 mm/min} \\ \mbox{Wire tension: } 20 ± 1 N \\ \mbox{WGR: } 0.32 mm \\ \end{array}$	

There is another big issue where electric isolation is needed between the DC power supply and wire-broken protection circuit. As the commercialized multi-wire saw system has the wire-broken protection function, there should be no transformation of voltage or current levels. Fig. 3 shows the waveform of wire-broken protection circuit when the DC power supply is applied on the silicon ingot and the wire.

After numerous trials, a certain formulation of conductive adhesive was introduced, which is suited to the silicon material and has good conductance as well. An important property is that it can be washed away by hot water in the cleaning line. Fig. 4 shows the experimental configuration.

Experiments have been carried out to investigate the fundamental experiment conditions by using mono crystalline Si ingot. 125 mm \times 125 mm (6") p-type (boron-doped) monocrystalline silicon ingots with a resistivity of 1.6–1.8 Ω cm are used as samples. The mixture of SiC and PEG is a coolant used as the industrial slurry for the wafer manufacturing process. In this case, with the demand for electrochemical grinding, it is also used as an electrolyte. WGR pitch distance is 320 μ m and the diameter of wire is 120 μ m, and the size of SiC is less than 15 μ m, hereby the thickness of the wafers is about 180 μ m.

3. Results and discussions

This study has concentrated solely on the effects of abrasive electrochemical slicing of silicon ingots. If the slicing is a two-step process, i.e., oxidation by electrolyte and removing the oxide by grinding, what we should do is to find the difference amongst the surface topography of multi-wire slurry, fixed abrasive and this



Silicon ingot

Fig. 4. Schematic view of electrical connecting method.

new approach. Moreover, the cutting rate, the total thickness variation (TTV) and even the profile bending rate (warp) of those important specifications should be improved due to this hybrid machining process.

As a preparatory study for slicing silicon blocks, the cutting rate is not the most important issue in this work. In fact, the feed rate is still as fast as 0.45 mm/min, which is better than the average level in the industry. The TTV is within 10 μ m, and the warp is also a little lower than that of the traditional multi-wire sawing production.

Hereby, experiments are mainly carried out to investigate the surface topography. A surface texture of a sliced wafer by three different types of multi-wire sawing, shown as Fig. 5, is evaluated over a length of 60 μ m. Two dots, i.e., red and blue are randomly selected from the image to generate the cross section line parallel to the actual feed direction. There are obvious surface micro-cracks or other damage on the wafer by using traditional multi-wire sawing methods which are shown in Fig. 5(a) and (b). The surface quality after slicing is better when the abrasive electrochemical operations are conducted as shown in Fig. 5(c). The maximum peak to valley height of the profile is 3.48 μ m, 2.86 μ m and 1.91 μ m, respectively. The surface roughness, *Ra*, is at best 0.32 μ m.

The difference in surface topography implies different cutting mechanisms. The even surface generated by using abrasive electrochemical method maybe attributed to "oxidation by electrolyte and removing the oxide by grinding". If this is the case, the "strong" electrolyte will lead to increase the cutting rate because of the anodic dissolution of silicon. Actually, PEG is only a weak electrolyte with low conductivity, and the "strong" electrolytes are not allowed to be introduced. This has caused the authors to think about the following queries:

• What is the abrasive electrochemical processing mechanism for slicing of silicon ingots?

• Is the passivation layer a single material or a mixture of several?

• Is there any similarity to ELID grinding?



Fig. 5. Sliced surface topography, (a) fixed abrasive, (b) slurry and (c) abrasive electrochemical sawing.

Firstly, the silicon atom possesses four valence electrons and therefore requires four bonds to fully saturate the valence shell. In the crystalline structure each silicon atom establishes bonds to its four neighbouring atoms, leaving no unsaturated bond behind. Due to the cut-grinding process, the surface of the silicon crystal atoms are missing and traps are formed as shown in Fig. 6(a). After anodic oxidation most interface states are saturated with oxygen atoms as a passive film (Fig. 6(b)), which can be removed by abrasives, then, the "fresh" surface appears again, which is the material removal mechanism inside of the slicing process.

Secondly, a properly passivated silicon surface is chemically stable, and all interface properties are constant. The silicon dioxide layers fulfil the chemical stability requirements. However, their surfaces and interface charges have an effect on the silicon surface potential barrier. The silicon covered by an ultra-thin (tunnelable) insulator (native SiO₂) layer has some peculiarities, i.e., connection between surface charge and the interface charge carrier density, which result in depletion or near intrinsic conditions on the silicon surface. Since passivation methods using organic molecules have been studied [7], we believe that the modification of surface potential by PEG is attractive as the possible passivation method during the slicing process. Further work will investigate the sliced surface elemental composition by X-ray photoelectron spectroscopy (XPS).

Surface passivation effects are strongly affected by the surface potential of silicon. Charging up the insulator surface, the previously discussed surface conditions can be altered, consequently the surface charge may have some passivating effect. Although this effect has no importance in the device technology because of short time duration and possible instabilities, it can be concluded that deposition of static charge is the appropriate treatment for surface passivation.

Finally, ELID grinding is an abrasive grinding process using electrochemical dressing. A typical ELID grinding system consists of wheel bond material, grinding fluid and a power supply. The metal-bonded abrasive wheel serves as the anode, and an electrode fixed at a small distance from the wheel serves as the cathode. The small interelectrode gap is supplied with grinding fluid and electrical current. The bonding material is electrolytically removed during ELID grinding, resulting in the reduction of wheel wear. It has been successfully used on surface grinding, cylindrical grinding, internal grinding, and centerless grinding [8]. Thereby, the only similarity between these two methods is the principle of electrochemical grinding, whilst the material removal mechanism is totally different.

In order to investigate the processing compatibility of this slicing method, the sliced wafers were sent to a solar cell plant for further photolithographic, doping and contact processing for the photoelectric transformation efficiency test. After texturing, the anti-reflectance is about 10% in the visible band, as shown in Fig. 7(a). Fig. 7(b) shows the 3D surface topography.

Minority carrier lifetime is quite important for the quality of the solar cell. Hereby, it has been measured before and after passivation, i.e., coated silicon nitride film. The range of minority



Fig. 6. (a) At the silicon surface silicon atoms are missing and unpaired valence electrons exist forming electrically active interface traps, and (b) after oxidation most interface states are saturated with oxygen bonds.

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Fig. 7. (a) Anti-reflectance, and (b) surface topography.



Fig. 8. Minority carrier lifetime (a) before, and (b) after passivation.



Fig. 9. (a) Silicon wafer, and (b) solar cell.

carrier lifetimes before passivation is from 1.32 µs to 1.95 µs as shown in Fig. 8(a), whilst after passivation it is from 26 µs to 64 µs as shown in Fig. 8(b).

Fig. 9 shows the solar cell samples in the average photoelectric transformation efficiency >17.5%. In comparison to the same silicon material sliced by using traditional multi-wire sawing method, the average photoelectric transformation efficiency is raised nearly one percent. It is to be noted that the improvement of surface quality is an important issue of solar cell production.

4. Conclusions

In retrospect, the last ten or twenty years have mainly dealt with the scaling up of wire saw technology. The currently employed slurry systems based on PEG, oil, or other glycol-based substances are well suited for today's applications. Improving the currently employed slurry system and working on the basic understanding of the cutting mechanisms are not only very challenging but also exceptionally exciting, due to the unusual numerous physical processes involved such as Non-Newtonian hydraulics, Thermodynamics, Solid State Physics along with new principles. Fixed abrasive, i.e., diamond coated wire has been used for several years to cut very hard and brittle materials such as sapphire, SiC single crystals, or various compound semiconductors. The main advantage of diamond wire over slurry is the possibility to significantly increase feed speeds. However, the surface microcracks or striae are still unavoidable and the very long cutting wire lengths required for solar wafering are still a challenge for the diamond wire manufacturers.

With the growing demand for larger and thinner wafers and increasing ingot lengths to be cut on wire saws, especially for the increase of wafer output per kg of silicon by reducing the kerf loss, whilst increasing the cutting speeds and maintaining the high quality requirements, abrasive electrochemical multi-wire slicing is possible to be a potential approach to face these challenges. In comparison to the existing sawing method, this technique obviously has several advantages, such as higher production rate, lower cost and better surface integrity, which are due to the different material removal mechanism of hybrid machining. What's more, better sub-surface integrity will be useful for production of large scale wafer handling and yield as well. Further work will be needed to identify the optimum processing parameters of this new slicing method. Very interesting question is the possibility of texturing wafers with this technique as slicing method, which is as yet a sealed book.

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