

A 2 Gb/s optical receiver with monolithically integrated MSM photodetector in standard CMOS process

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A monolithically standard complementary-metal-oxide-semiconductor (CMOS) optical receiver with a metal-semiconductor-metal (MSM) photodetector is presented in this paper. An active-feedback transimpedance amplifier (TIA) with negative Miller capacitance is used to increase the bandwidth of the receiver. The MSM photodetector with high responsivity provides higher sensitivity for the optical receiver. The optical receiver implemented in chartered 0.35 μm process achieves a 1.7 GHz bandwidth due to the low capacitance of the MSM photodetector. 2 Gb/s optical data are successfully transmitted with a bit-error rate of 10^{-9} at an optical power of -15 dBm. The power consumption of the receiver is 94 mW under a single 3.3 V supply.

optical receiver, TIA, MSM photodetector, CMOS

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Communication systems have always been the subject of a lot of researches. Today however, the transmission of data is becoming the performance limiting action. To enhance the performance of the communication, an optical communication system is researched to solve problems in present communication system. Nowadays, the research of optical receiver has got much progress [1,2].

In recent years, a lot of researches of hybrid integration optical receiver were reported [3,4]. Because the cost of packaging and fabricating are reduced greatly in standard CMOS process, much more attention of optical receiver has been attached to the research of monolithically integrated CMOS optical receivers for low cost. For example, an 1 Gb/s optical receiver with a -6 dBm sensitivity for $\lambda=850$ nm in 0.35 μm standard CMOS process was first reported by Bell laboratory [5]. Nevertheless, the sensitivity of the silicon-based, standard CMOS optical receiver is still a bit low because of the disadvantage of silicon material. Therefore the low responsivity problem of silicon detector is to need solution urgently. In order to solve this problem, some

researches of high responsive MSM photodetector were reported. Li realized a MSM photodetector with the responsivity of 0.118 A/W in Si-based process [6]. Robert reported a MSM polysilicon photodiode with 0.35 A/W responsivity in 0.35 μm CMOS process [7].

In this paper, a monolithically integrated optical receiver with a MSM photodetector is presented. Generally, the sensitivity of the receiver could be improved by increasing the responsivity of the photodetector. In order to solve the problem of the low responsivity, a MSM photodetector is adopted in this optical receiver. Since Schottky diode is a major-carrier device, a MSM photodetector based Schottky diode has higher responsivity and better frequency characteristic. Besides all, the MSM photodetector has an advantage of low capacitance per unit area. In addition, an active-feedback TIA is adopted in the receiver in order to improve the bandwidth of the receiver.

1 The design of the MSM photodetector in standard CMOS process

A MSM photodetector integrated in standard CMOS

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process is presented in this part. The MSM photodetector fabricated in commercial CMOS process have three advantages: high responsivity, wide bandwidth and low cost. It is shown that the MSM photodetector in standard CMOS process achieves a bandwidth of 919 MHz and a responsivity of 0.21 A/W [8].

The structure of the MSM photodetector is shown in Figure 1, where Psub represents P-type substrate guarding, Nwell represents N-type well, SBDCOMP represents Schottky implantation region only for Schottky diode. The MSM photodetector includes two back-to-back Schottky diodes, which are composed of Nwell and metal1. The GND guarding outside Nwell is just used to eliminating slow photo-generated carriers from P-type substrate. The Schottky diode is designed to interdigital structure, which is used to improve the bandwidth and responsivity of the photodetector. The finger width is 0.8 μm , and the finger spacing is 0.5 μm .

The MSM photodetector is symmetrical, So IN1 and IN2 are equivalent, no definition in anode and cathode. Thus, the operating principle of the MSM photodetector is different from that of the p-n junction diode photodetector. When the MSM photodetector is under incident light illumination, photo-generated holes will diffuse to electrode in forward-biased diode while photo-generated electrons will diffuse to electrode in reverse-biased diode. The MSM photodetector microphotograph enlarged a thousand times is displayed in Figure 2, and the area of the photodetector is 50 $\mu\text{m} \times 50 \mu\text{m}$.

2 The front-end circuit of the receiver

The architecture of the optical receiver is shown in Figure 3, which integrates two MSM photodetectors, a differential active-feedback TIA with negative Miller capacitance, three stage limiting amplifiers and an output buffer. Two MSM

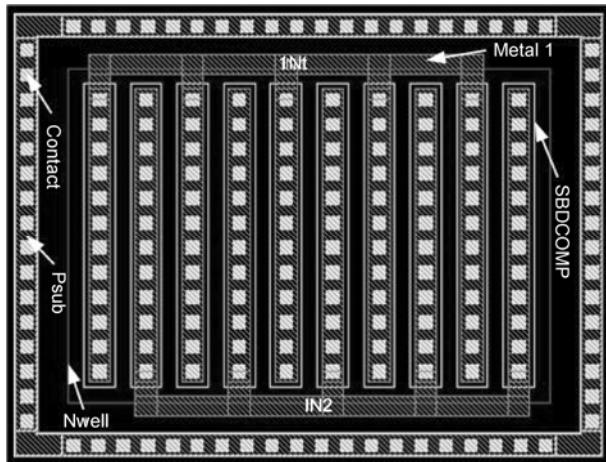


Figure 1 The structure of the MSM photodetector.

photodetectors are all the same. One generates photo currents for the differential TIA, while another dummy MSM photodetector could boost the bandwidth of the optical receiver [9]. The fully differential TIA converts photo current into differential voltage, and three stage limiting amplifiers further increase the voltage signal swing. For testing purpose, an output buffer is used to drive the voltage to the test equipment.

2.1 Transimpedance amplifier

To alleviate bandwidth degradation caused by the capacitance of the photodiode, an active-feedback TIA with negative Miller capacitance is adopted in this paper. A regulated cascode (RGC) stage has often been used to increase bandwidth of the receiver. However, this structure will degrade the sensitivity of the receiver due to relatively large input noise current. Conventional shunt-feedback TIA with common source gain stage contributes lower input noise current, but the bandwidth and the input noise trade off seriously. The schematic of the proposed TIA is shown in Figure 4. This TIA is composed of two stage common-source amplifiers, an active-feedback differential pair and two shunt-feedback resistors. The conversion gain of the TIA could be expressed as

$$A_Z = \frac{\frac{g_{m3}g_{m7}}{g_{m1}g_{m5}} + R_F}{\frac{g_{m3}g_{m7}}{g_{m1}g_{m5}} + 1 + \frac{g_{m9}}{g_{m1}}} \approx \frac{R_F}{1 + \frac{g_{m9}}{g_{m1}}}. \quad (1)$$

The bandwidth of the TIA can be approximated as

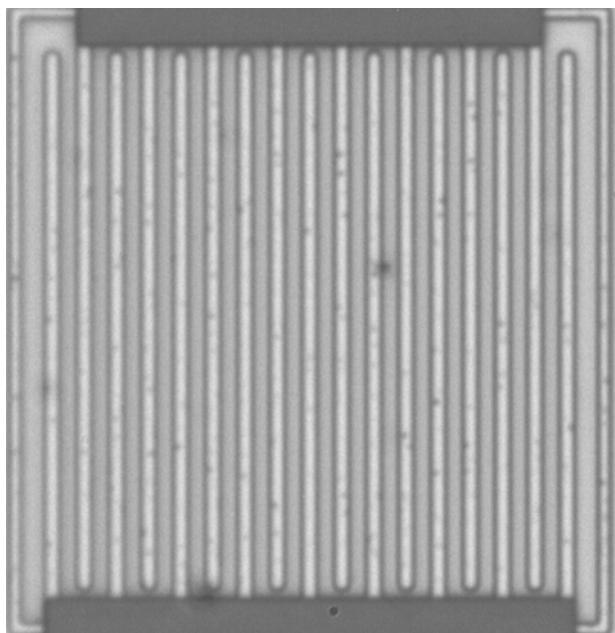


Figure 2 The MSM photodetector microphotograph enlarged a thousand times.

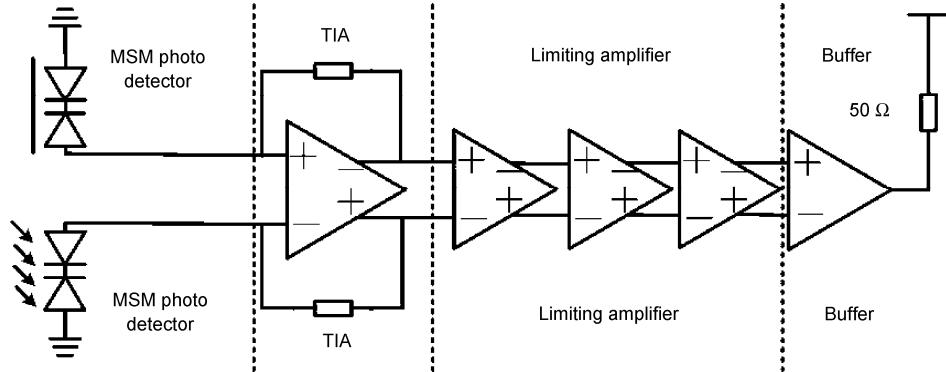


Figure 3 The architecture of the optical receiver.

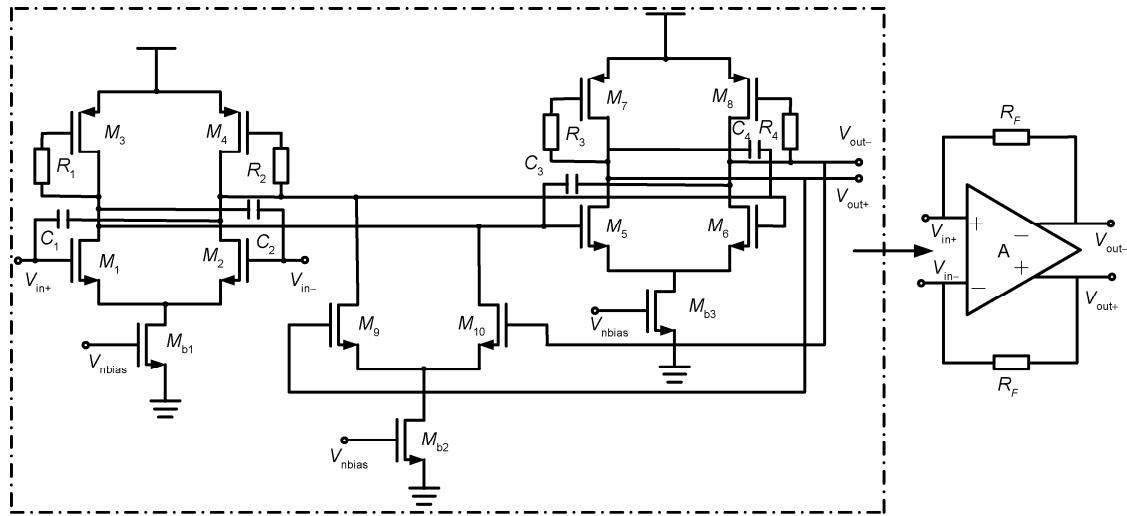


Figure 4 The schematic of the active-feedback TIA.

$$f_{-3\text{dB}} = \frac{A}{2\pi R_F C_{\text{in}}}, \quad (2)$$

where A is the open loop gain of the core amplifier, and C_{in} includes the input capacitance of the TIA and the capacitance of the MSM photodetector. A $2\text{k}\Omega R_F$ is chosen to provide a moderate transas impedance gain as a compromise between the input noise current and the bandwidth of the TIA. In order to enhance the bandwidth of the TIA, active feedback is used to remove the gain peaking. In addition to active feedback, each stage of the common source employs folded active inductive peaking and negative Miller capacitance. The capacitors C_1 , C_2 , C_3 and C_4 cancel the effect of gate-drain and gate-source capacitors of M_1 , M_2 , M_3 and M_4 . The resistors R_1 , R_2 , R_3 and R_4 used to generate folded active inductors can be implemented by linear transistor resistors. Finally the TIA provides a conversion gain of about 60 dB for a trade-off consideration, and the bandwidth of the TIA is about 2 GHz.

2.2 Limiting amplifier and output buffer

The architecture of one stage limiting amplifier is shown in

Figure 5(a). In three stage limiting amplifiers, the gain of every stage is equal to e in order to alleviate the bandwidth of multistage amplifier decreasing. In addition, folded active inductors [10] are applied in the limiting amplifier to increase its bandwidth. The conventional resistors in folded active inductor are replaced by the linear transistor resistors. Usually, the poly silicon resistor in folded active inductor occupies a lot of area, and it is easily influenced by process conditions. The linear transistor resistors could save a lot of area compared with the poly silicon resistors. The 3 dB bandwidth of three limiting amplifiers is about 4 GHz, and the total gain is about 26 dB.

The high bandwidth of the differential to single-ended output buffer is realized by the two n-metal-oxide-semiconductor (NMOS) diodes in parallel with the current mirror in Figure 5(b). The differential to single-ended output buffer has an advantage to not decrease gain of the receiver compared with the conventional buffer. The bandwidth of the output buffer is 5 GHz, and its gain is about -1 dB.

3 The simulation and experimental results

Using the fabricated CMOS integrated optical receiver,

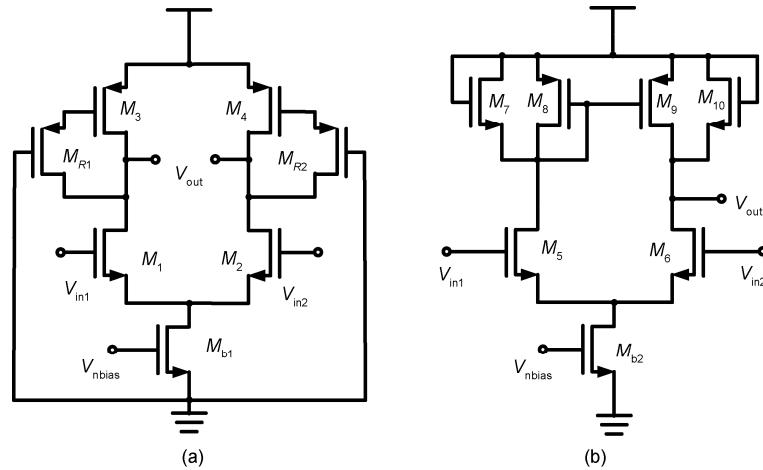


Figure 5 (a) The schematic of one stage limiting amplifier; (b) the schematic of the output buffer.

optical data transmission experiments were performed. No additional masks or reflective coatings have been used to improve the photodiode performance. The chip microphotograph enlarged fifty times is shown in Figure 6, where the core size is $1150 \mu\text{m} \times 320 \mu\text{m}$. The total power of the chip is 94 mW under a single 3.3 V supply. The simulated alternating current (AC) response of the receiver is shown in Figure 7, which is obtained by Cadence Spectre. The optical receiver provides a transimpedance gain of 85 dB, and the overall 3 dB bandwidth is 1.9 GHz.

Agilent network analyzer E5062A, Agilent ParBERT (parallel bit error ratio tester) 81250, New Focus 10 Gb/s

VCSEL (vertical cavity surface emitting laser) and Agilent wide bandwidth oscilloscope 86100C were used to measure the receiver performance. The measured frequency response result shows the receiver achieves 1.7 GHz 3 dB bandwidth in Figure 8, which is basically consistent with the simulated result. The gain peaking in test results is induced by parasitic resistors of active inductors. The experimental bandwidth is decreased due to the parasitic capacitance of testing PCB board and testing equipment. Figure 9 shows the measured eye diagram at 2 Gb/s and -15 dBm data rates for $2^{31}-1$ pseudorandom bit sequence (PRBS). The eye diagram is open widely, and its amplitude is about 120 mV.

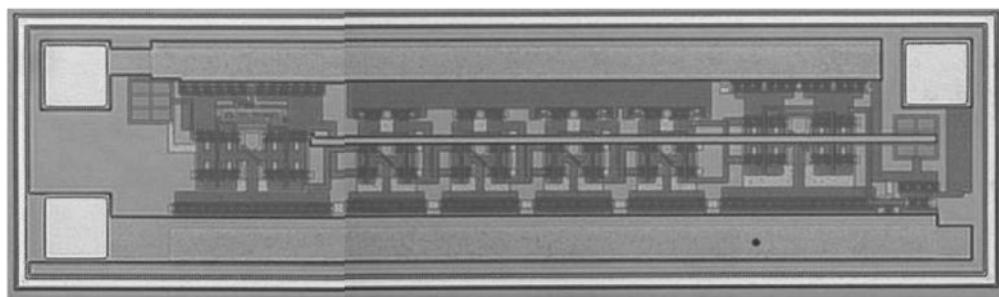


Figure 6 The chip microphotograph enlarged fifty times.

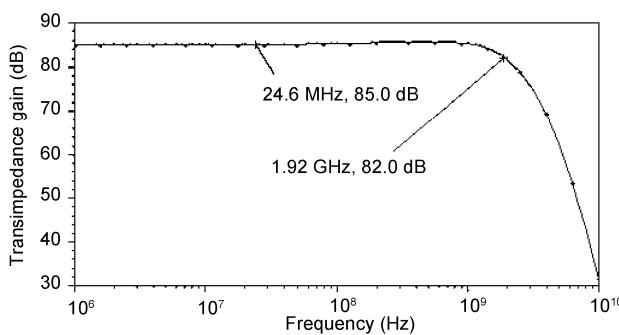


Figure 7 The simulated frequency response of the receiver.

4 Conclusion

An optical receiver with monolithically integrated MSM photodetector has been implemented in an unmodified 0.35 μm CMOS process. The MSM photodetector and active-feedback TIA are adopted to increase the bandwidth and sensitivity of the optical receiver. The receiver provides a conversion gain of 85 dB and a 3 dB bandwidth of 1.7 GHz. Using the monolithically integrated optical receiver, a data rate of 2 Gb/s is achieved by the receiver with an optical power of -15 dBm . The measured results show

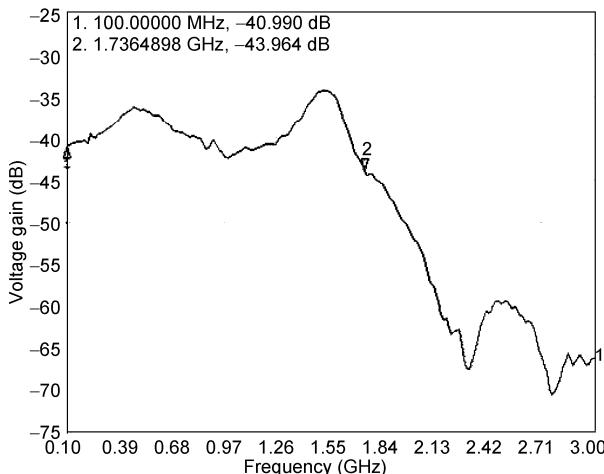


Figure 8 The measured frequency response of the receiver.

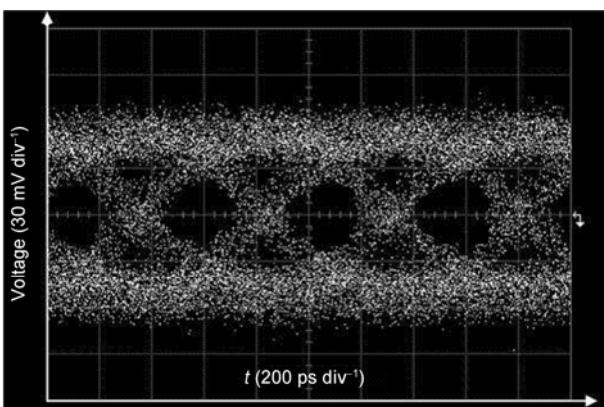


Figure 9 The measured eye diagram at 2 Gb/s.

that the optical receiver with MSM photodetector and active-feedback TIA is promising for low-cost optical com-

munication system applications.

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