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A novel voltage-type sense amplifier for low-power nonvolatile memories

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Abstract Based on the requirements of the nonvolatile memories embedded in ultra low-power RFID transponders, a novel voltage-type sense amplifier is designed to achieve both the reduced reading power and the improved reliability. Compared to the conventional voltage-type sense amplifier, the additional capacitor and current limiter are introduced in the novel voltage-type sense amplifier to reduce the reading power and to improve the reading reliability. The simulations show that the reading power and reliability of our voltage-type sense amplifier are superior to the previously reported voltage-type sense amplifier without speed loss but with only a little increased area. A testing chip has been fabricated based on 0.18 μm EEPROM technology to verify the design. The novel voltage-type sense amplifier can be implemented to the low-power nonvolatile memory embedded in RFID transponder.

Keywords sense amplifier, nonvolatile memory, transponder, low-power

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1 Introduction

Embedded nonvolatile memories (NVM) are essential in radio-frequency identification (RFID) transponders which have been widely used around the world. The reading and writing power are usually the limit factors for the operations of low-power transponders [1, 2]. To increase RFID reading distance, the power of the sense amplifier of the embedded NVM must be as low as possible [3]. Meanwhile reliability of sense amplifiers must be enhanced for reliable operations of transponders.

Currently, current-type sense amplifiers have been widely adopted for NVM reading rather than voltage-type sense amplifiers due to the higher speed and reliability of current-comparing methods [4]. However, current-type sense amplifiers usually dissipate larger current and power than voltage-type sense amplifiers [4–6], which is inapplicable to the low-power RFID transponders. Several voltage-type sense amplifiers have been reported to achieve the reduced NVM reading current [2, 7, 8], but they suffer from the reading reliability at low power supply and the high reading current.

In this paper, a novel voltage-type sense amplifier is designed to achieve the lower reading current/power and the higher reading reliability without speed degradation compared to the conventional voltage-type sense amplifier. An additional capacitor is used to reduce the reading current and a negative feedback loop with a current limiter is used to improve the reading reliability. Moreover, the capacitor and the

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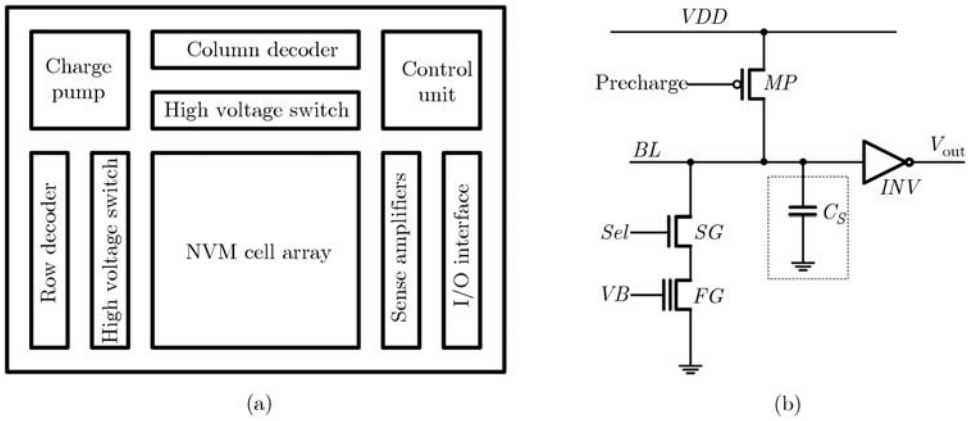

Figure 1 (a) Schematic chart of an EEPROM system; (b) the circuit structure of a typical voltage-type sense amplifier.

current limiter are adjustable to meet power and reliability constraints. A testing chip containing this improved voltage-type sense amplifier and floating-gate memory cells has been implemented in 0.18 μm EEPROM process. Simulations and measurements show that the proposed sense amplifier has better performance.

2 Nonvolatile memory and sense amplifier

A typical EEPROM-type NVM circuit scheme is shown in Figure 1(a). The NVM cell array is utilized to store data. Since evolution of floating-gate devices meets many limits [9], low-power design on circuit level is the best solution for RFID applications currently. The control unit, row and column decoders, and high-voltage switches are to direct logic operations. The charge pump produces a high voltage for writing operations. The sense amplifiers and input/output (I/O) interfaces are for reading operations and sending data out.

A typical voltage-type sense amplifier is shown in Figure 1(b). Voltage-type sense amplifiers perform reading through examining whether the memory cell can discharge a capacitive node. When VDD becomes lower, discharging time will increase. Then reading power of the voltage-type sense amplifiers reported in [2] and [7] will decrease very slowly as VDD decreases, because inverters are connected to the discharged nodes directly. Therefore, reliability problems such as the reading error will emerge in the conventional voltage-type sense amplifiers [2, 8]. Besides, the reduced reading current/power is still expected to meet the requirements of low-power RFID transponders.

Based on the above mentioned issues, a novel voltage-type sense amplifier with lower power and higher reliability has been developed as shown in Figure 2(a). The corresponding operation timing is shown in Figure 2(b). In the improved voltage-type sense amplifier, block A represents a selected reading path, including a floating gate FG and a selecting gate SG. The word line WL is controlled by the decoders, and the terminal VB is driven by a voltage between the two thresholds of memory cells. The first voltage on bit line BL is reset to zero by the $INIT$-controlled transistor MN. Then the reading pulse RP which is generated by the control unit of EEPROM rises from zero to VDD at the moment MN has been shut down. If FG is storing "1", the voltage on BL will keep on VDD. In contrast to this, if FG is storing "0", the BL will be discharged quickly from VDD to zero by FG.

Block B in Figure 2(a) represents a new additional current limiter from outside for $M1$ and MF corresponding to the typical voltage-type sense amplifier. Sufficient low reference current $I_{\rm ref}$ can be set as long as it is larger than the leakage current on BL while FG is storing "1". The negative feedback loop composed of transistor $M2$ and inverter $INV1$ is used for keeping the voltage on BL while FG is storing "1". And transistor $M1$ is for keeping the current through $M2$ smaller than cell current while FG is storing "0" and then increasing reading reliability and speed.

Transistors $M3, M6$ and inverter $INV2$ in Figure 2(a) constitute output stage of the proposed sense amplifier. $INV3, INV4$ and switch S form an outer latch. Signal EN makes $M4$ and $M5$ cut-off before

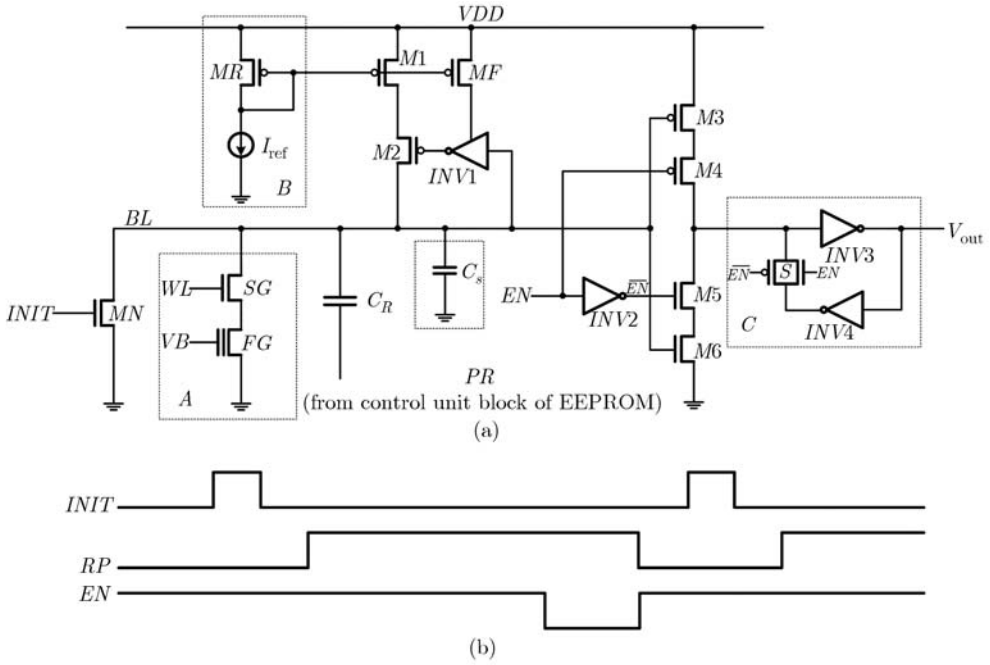

Figure 2 (a) The circuit structure of the novel voltage-type sense amplifier (Blocks A, B and C are not integral parts of the SA); (b) the operation timing diagram of the novel voltage-type sense amplifier.

the voltage on BL has become stable, and meanwhile keeps switch S closed. Inverters $INV3$ and $INV4$ shall keep the previous status on V_{out}. After the voltage on BL becomes stable, signal EN will make $M4$ and $M5$ turn-on, and make S open. Then the output stage will send new data to V_{out}. These operations can avoid current increasing in inverters when discharging time becomes longer.

An additional capacitor C_R called "reading capacitor" is introduced in the designed sense amplifier and C_S represents parasitic capacitance on BL. Due to charge sharing effect between C_R and C_S, the following condition should be satisfied to ensure the voltage on BL higher than $VDD/2$ (threshold of inverters) while reading "1".

$$C_R \geqslant C_S. \tag{1}$$

If FG is storing data "0", the average current consumed by the sense amplifier can be calculated by

$$I_R = I_{\text{ref}} + \frac{VDD}{T} C_R, \tag{2}$$

T denotes the reading period. The value of C_S has no effect on I_R. Because BL will be connected to ground by FG storing "0" when RP goes high from low, the voltage on C_S does not change and so it has no charge loss. The smaller C_R is, the smaller I_R is. So the overall power of the sense amplifier is adjustable via C_R.

3 Verification

Firstly, simulations have been performed to compare the circuit performances of the newly designed voltage-type sense amplifiers with the previously reported voltage-type sense amplifiers [2, 7, 8], including the reading current/power, reading reliability and the sensing time. The critical design parameters are listed in Table 1. Simulated control signals and waveforms on BL and V_{out} are shown in Figure 3.

Figure 4 shows the comparisons of the average reading currents, indicating that the novel voltage-type sense amplifier costs the lowest power in the target range of VDD and read cycle. Meanwhile, the simulations also indicate that reading error will occur if VDD is lower than 1.25 V or 1.5 V for the sense amplifiers reported in [2, 8], but the reading error point is lower than 1 V for the newly designed sense

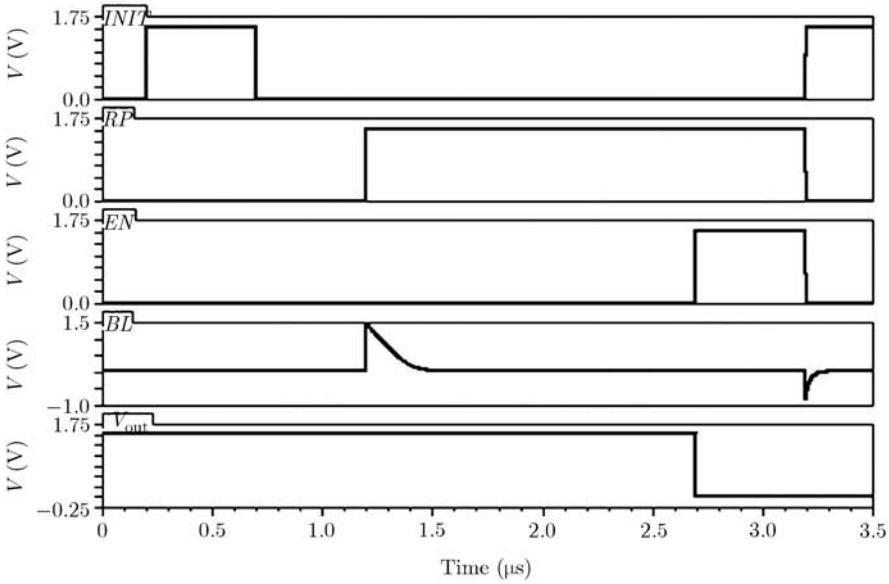

Figure 3 Simulated waveforms of the new deigned voltage-type sense amplifier.

Table 1 Main design parameters

WL	VB	I_{ref}-III	I_{ref}-IV	C_R	$(W/L)_{\text{precharge}}$
VDD-V_{tz}	VDD	0.6 μ	0.1 μ	0.3 p	0.5 μ/1 μ

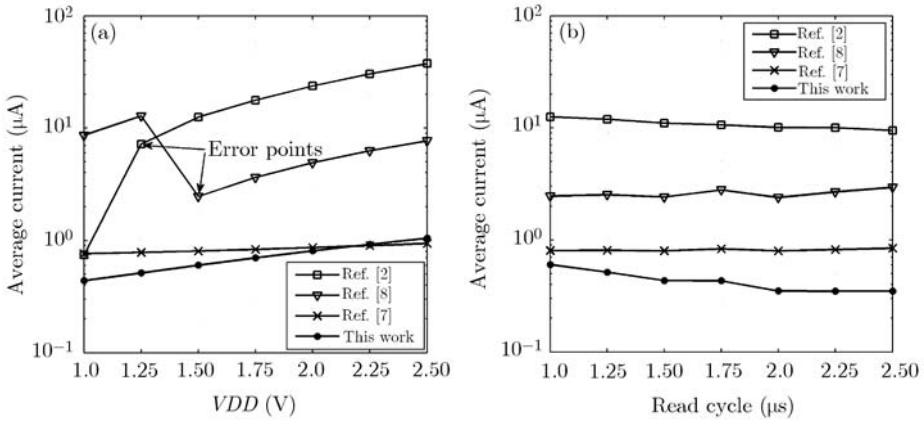

Figure 4 Simulation results. (a) Current versus VDD @ 1 MHz; (b) current versus read cycle @ VDD=1.5 V.

amplifier. The simulations also show that for the sense amplifier reported in [7], I_{ref} cannot be too small, otherwise read cycle will become very long for FG storing "1". In contrast to this, similar issues will not occur for the improved sense amplifier. Therefore, quite small I_{ref} can be set to achieve the low reading current/power.

Simulation results in Figure 5 show the variation of BL sensing time versus reference current or parasitic cap on BL, where BL sensing time denotes the time in which the voltage on BL reaches the threshold of inverters from its initial status. BL sensing time is critical for the operating speed of voltage-type sense amplifiers. It can be seen that BL sensing time for the sense amplifier previously reported in [7] varies seriously with I_{ref} or C_S, but it rarely varies with them in the improved voltage-type sense amplifier.

Moreover, a testing chip has been implemented based on 0.18 μm EEPROM process as shown in Figure 6. The testing chip includes the new designed voltage-type sense amplifier array and a floating-gate memory cell array. Since EEPROMs always work in byte mode, eight sense amplifiers are required to read a byte simultaneously. Each reading capacitor C_R is about 0.3 pF (18 μm×18 μm for MIM cap), and parasitic capacitance C_S is less than 0.1 pF in this design. It is only a little area cost (less than 3%) in the whole chip.

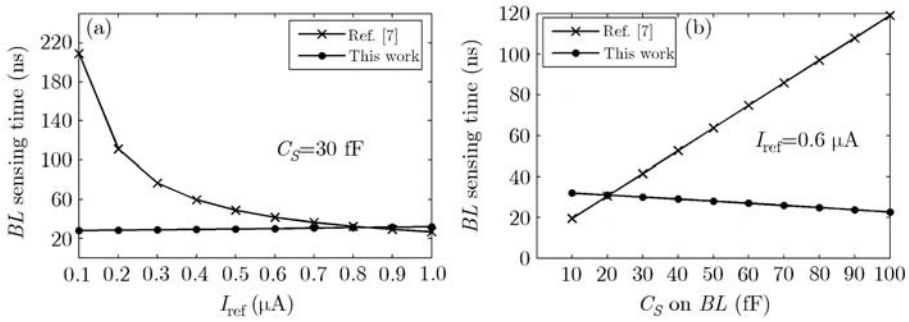

Figure 5 Simulated BL sensing time @ VDD=1.5 V. (a) BL sensing time versus reference current; (b) BL sensing time versus parasitic capacitance on BL.

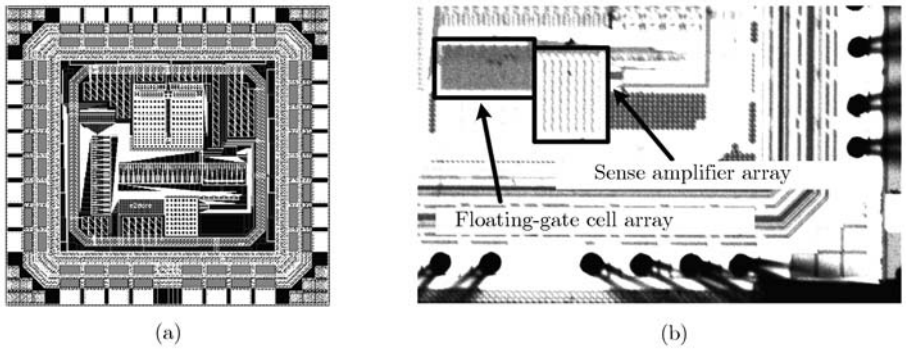

Figure 6 Implemented testing chip fabricated in SMIC 0.18 μm EEPROM process. (a) Layout of the whole chip; (b) chip photograph.

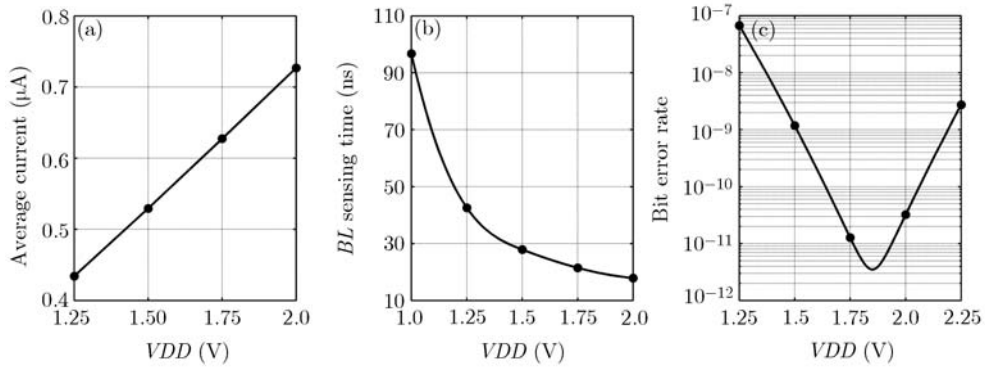

Figure 7 Measured results versus VDD. (a) Average current @ 640 KHz; (b) BL sensing time; (c) bit error rate @ 640 KHz.

Table 2 Comparisons among voltage-type sense amplifiers

1.5 V@640 kHz	Ref. [2]	Ref. [8]	Ref. [7]	This work
Current (μA)	5	3.6	>0.6	0.53
Error point (V)	1.25	1.5	<1	<1

Figure 7 shows the measured results of the novel voltage-type sense amplifier in the testing chip during reading operations at different VDD. Reading operations were measured at frequency of 640 kHz. The average current increases linearly with the power supply as shown in Figure 7(a). It has been assumed that the overall power of the testing chip is consumed by sense amplifiers. Therefore, the measured current shown in Figure 7(a) is a little larger than the value calculated by formula (2) because other blocks such as decoders and control units also contribute to the overall power. The values of BL sensing

time and bit error rate are shown in Figure 7(b) and (c) respectively. By these curves right working points can be chosen for sense amplifiers to meet RFID system requirements. Finally comparisons on power and reliability among voltage-type sense amplifiers are shown in Table 2. It should be noted that the current consumption of the proposed voltage-type sense amplifiers can be further reduced if a reduced C_R is designed.

4 Conclusions

A novel voltage-type sense amplifier is designed for the application of nonvolatile memory in ultra low-power RFID passive transponders. In the novel voltage-type sense amplifier, an additional capacitor and a current limiter are introduced into the typical voltage-type sense amplifier to achieve the low reading current/power and high reading operation reliability. The simulations show that the new designed voltage-type sense amplifier has lower reading error voltage point and the reading current in the target range of VDD and read cycle than the previously reported voltage-type sense amplifier. A testing chip containing this sense amplifier has been manufactured in 0.18 μm EEPROM process. The measurement results verified the feasibility of the designed novel voltage-type sense amplifier for the application of NVM applicable in RFID transponders.

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